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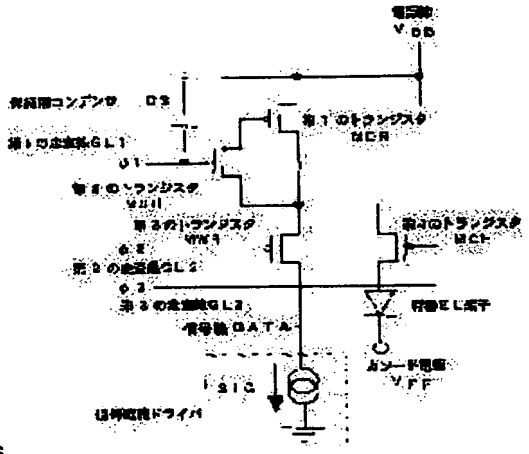
(54) ACTIVE MATRIX TYPE OLED DISPLAY DEVICE AND ITS DRIVING CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an OLED (organic light emitting diode) driving pixel circuit having satisfactory display performance.
SOLUTION: In this pixel circuit, four transistors are constituted in a pixel and after first and second scanning lines GL1, GL2 which are connected respectively to the gate electrode of a second transistor MSH and that of a third transistor MWR are made active and the gate electrode and the drain electrode of a first transistor MDR are made to be in conduction state via the second transistor MSH and a current having a value corresponding to a video signal is made to flow from a power source to a signal line through the first and third transistors MDR, MWR and the first scanning line GL1 is made inactive, the second scanning line GL2 is made inactive and thereafter a third scanning line GL3 which is connected to the gate electrode of a fourth transistor MCH is made active and a current having a value corresponding to the video signal is made to flow through an OLED through the fourth transistor MCH.



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CLAIMS

[Claim(s)]
[Claim 1] In the display with which a unit pixel consists of two or more transistors and OLED components The 1st transistor by which the source electrode was connected to the power source into said unit pixel, The capacitor by which one electrode was connected to said power source, and the electrode of another side was connected to the gate electrode of said 1st transistor, Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. Another side of a source electrode or a drain electrode is connected to the gate electrode of said 1st transistor. Either the 2nd transistor and source electrode by which the gate electrode was connected to the 1st scanning line, or a drain electrode is connected to the drain electrode of said 1st transistor. The 3rd transistor by which another side of a source electrode or a drain electrode was connected to the signal line, and the gate electrode was connected to the 2nd scanning line, Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. The active-matrix mold OLED display characterized by having the 4th transistor by which another side of a source electrode or a drain electrode was connected to the OLED component, and the gate electrode was connected to the 3rd scanning line [claim 2] In the display with which a unit pixel consists of two or more transistors and OLED components The 1st transistor by which the source electrode was connected to the power source into said unit pixel, The capacitor by which one electrode was connected to said power source, and the electrode of another side was connected to the gate electrode of said 1st transistor, Either a source electrode or a drain electrode is connected to the gate electrode of said 1st transistor. The 3rd transistor by which either the 2nd transistor and source electrode by which the gate electrode was connected to the 1st scanning line, or the drain electrode was connected to the signal line, and the gate electrode was connected to the 2nd scanning line, Either the 4th transistor and source electrode by which either the source electrode or the drain electrode was connected to the OLED component, and the gate electrode was connected to the 3rd scanning line, or a drain electrode It connects with the drain electrode of said 1st transistor. Another side of a source electrode or a drain electrode Another side of the source electrode of said 2nd transistor, or a drain electrode, The active-matrix mold OLED display characterized by having the 5th transistor connected to another side of another side of the source electrode of said 3rd transistor, or a drain electrode and the source electrode of said 4th transistor, or a drain electrode [claim 3] Claim 1 by which it is being [it / the conductivity type with which said 2nd and 3rd scanning lines are common with a conductivity type, and said the 3rd transistor and 4th transistor differed from each other] characterized, and an active-matrix mold OLED display [claim 4] according to claim 2 said the 3rd transistor and said 4th transistor of another side are unjust when one side is switch-on -- a connoisseur -- the active-matrix mold OLED display [claim 5] according to claim 3 by which it is having-threshold property which will be in condition characterized Said transistor is an active-matrix mold OLED display [claim 6] given in four from claim 1 characterized by being the thin film transistor component which used polish recon. Said 1st transistor is an active-matrix mold OLED display [claim 7] according to claim 5 characterized by being the transistor of a hole conductivity type. Said 2nd transistor is claim 5 characterized by connecting to a serial two or more transistor components by which the gate electrode was connected to the common gate line, and changing, and an active-matrix mold OLED display [claim 8] given in six. An active-matrix mold OLED indicating equipment given in seven from claim 5 to which at least one of the transistor components used for

the circuit for vertical scannings or level drive circuit of an active-matrix mold OLED indicating equipment is characterized by being formed in the transistor component and coincidence in a pixel [claim 9] Said vertical-scanning circuit is an active-matrix mold OLED display [claim 10] according to claim 8 characterized by including three different pulse width and the circuit which generates the scan wave which has a phase from one output of the shift register of the exterior or the interior. Said level drive circuit is claim 8 characterized by having a charge circuit for intercepting the current corresponding to said video signal, and making said signal line into fixed potential in some periods of a vertical-scanning period, and an active-matrix mold OLED display [claim 11] given in nine. An active-matrix mold OLED display given in ten from claim 1 characterized by change of the luminescence brightness between said adjoining pixels being a maximum of 2% [claim 12] The display for personal digital assistants characterized by using an active-matrix mold OLED indicating equipment given in 11 terms from claim 1 [claim 13] Large-sized television characterized by using an active-matrix mold OLED indicating equipment given in 11 terms from claim 1 [claim 14] The highly minute monitor characterized by using an active-matrix mold OLED display given in 11 terms from claim 1 [claim 15] In the display with which a unit pixel consists of two or more transistors and OLED components By activating the 1st scanning line and 2nd scanning line, the 1st gate electrode and drain electrode of a transistor After making it switch-on through the 2nd transistor, letting said the 1st transistor and 3rd transistor pass and passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive Said 2nd ** after holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line] The drive approach of the active-matrix mold OLED display characterized by activating the 3rd scanning line, letting the 4th transistor pass, and passing the current of the value corresponding to said video signal to said OLED after making **** inactive and making said 2nd scanning line inactive [claim 16] In the display with which a unit pixel consists of two or more transistors and OLED components While activating the 1st scanning line and 2nd scanning line and making the gate electrode of the 1st transistor, and the drain electrode of the 5th transistor into switch-on through the 2nd transistor Impress predetermined bias voltage to the gate voltage of the 5th transistor, and it lets said 1st transistor, the 3rd transistor, and the 5th transistor pass. After passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], After making said 2nd scanning line inactive and making said 2nd scanning line inactive, activate the 3rd scanning line and it lets the 4th transistor pass. The drive approach of the active-matrix mold OLED display characterized by passing the current of the value corresponding to said video signal to said OLED [claim 17] In the display with which a unit pixel consists of two or more transistors and OLED components By activating the 1st scanning line and 2nd scanning line, the 1st gate electrode and drain electrode of a transistor After making it switch-on through the 2nd transistor, letting said the 1st transistor and 3rd transistor pass and passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], Activate said 2nd scanning line to inactive and the 4th transistor to the 3rd transistor, and it lets the 4th transistor pass. The drive approach of the active-matrix mold OLED display characterized by passing the current of the value corresponding to said video signal to said OLED [claim 18] In the display with which a unit pixel consists of two or more transistors and OLED components While activating the 1st scanning line and 2nd scanning line and making the gate electrode of the 1st transistor, and the drain electrode of the 5th transistor into switch-on through the 2nd transistor Impress predetermined bias voltage to the gate voltage of the 5th transistor, and it lets said 1st transistor, the 3rd transistor, and the 5th transistor pass. After passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], Activate said 2nd scanning line to inactive and the 4th transistor to the 3rd transistor, and it lets the 4th transistor pass. The drive approach of the active-matrix mold OLED display characterized by passing the current of the value corresponding to said video signal to said OLED [claim 19] In the display with which a unit pixel consists of two or more transistors and OLED components Either a source electrode or a drain electrode is connected to the gate electrode of the 1st transistor by which the source electrode

was connected to the power source. The electrical potential difference of the 1st scanning line connected to the gate electrode of the 2nd transistor by which another side of a source electrode or a drain electrode was connected to the drain electrode of said 1st transistor said 2nd transistor is unjust -- a connoisseur, after making it inactive so that it may be in a condition Either a source electrode or a drain electrode is connected to the drain electrode of the 1st transistor. The electrical potential difference of the 2nd scanning line with which it connected with the signal line and another side of a source electrode or a drain electrode was connected to the gate electrode of the 3rd transistor It is made inactive. said 3rd transistor is unjust -- a connoisseur -- so that it may be in a condition Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. The electrical potential difference of the 3rd scanning line with which another side of a source electrode or a drain electrode was connected to the gate electrode of the 4th transistor connected to the OLED component The drive approach of the active-matrix mold OLED display characterized by activating as [be / in switch-on / said 4th transistor component] [claim 20] In the display with which a unit pixel consists of two or more transistors and OLED components Either a source electrode or a drain electrode is connected to the gate electrode of the 1st transistor by which the source electrode was connected to the power source. The electrical potential difference of the 1st scanning line connected to the gate electrode of the 2nd transistor by which another side of a source electrode or a drain electrode was connected to the drain electrode of said 1st transistor said 2nd transistor is unjust -- a connoisseur, after making it inactive so that it may be in a condition Either a source electrode or a drain electrode is connected to the drain electrode of the 1st transistor, and another side of a source electrode or a drain electrode is connected to a signal line. The gate electrode of the 3rd transistor, Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. The electrical potential difference of the 2nd scanning line with which another side of a source electrode or a drain electrode was connected to the gate electrode of the 4th transistor connected to the OLED component said 3rd transistor is unjust -- a connoisseur -- the drive approach [claim 21] of the active-matrix mold OLED display characterized by being in a condition and making it said 4th transistor component be in switch-on In the indicating equipment with which a unit pixel consists of two or more transistors and OLED components, in either a source electrode or a drain electrode, it connects with the drain electrode of said 1st transistor, and another side of a source electrode or a drain electrode The drive approach of claim 20 characterized by impressing predetermined bias voltage to the gate electrode of the 5th transistor connected to another side of another side of another side of the source electrode of said 2nd transistor, or a drain electrode, the source electrode of said 3rd transistor, or a drain electrode and the source electrode of said 4th transistor, or a drain electrode, and an active-matrix mold OLED display given in 21 [claim 22] Said both predetermined bias voltage is the drive approaches of claims 16 and 18 characterized by setting up said the 1st transistor and 5th transistor so that it may operate in a saturation region, and an active-matrix mold OLED display given in 21.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the new display aiming at improvement in display quality, and the drive approach about an active-matrix mold OLED display. (OLED is the abbreviated name of organic lighting emission diode.)
[0002]
[Description of the Prior Art] The circuit of the pixel cel of the conventional active-matrix mold OLED display The 1st transistor (it expresses also the transistor T1 for switching hereafter) is prepared in the intersection of wiring spread around in all directions. Connect the gate electrode to the scanning line (it is also called a gate line), and a drain electrode (or source electrode) is connected to a signal line (it is also called a drain wire or a source line). A source electrode (or drain electrode) is connected to the gate electrode of the 2nd transistor. Said 2nd transistor (it expresses also the transistor T2 for a drive hereafter) a source electrode (or drain electrode) -- a current supply source line (a following and power-source line --) It connects for expressing also power-source Rhine, Vdd, an anode line, and an anode line. A drain electrode (or source electrode) is connected to the anode electrode (or cathode electrode) of an OLED component, and it has the structure where the electrode of another side of an OLED component turns into a cathode electrode (or anode electrode). The equal circuit is shown in drawing 25 (A).
[0003] As mentioned above, the active-matrix method with which the thing whose at least two transistors are need is used for the OLED panel is for having to satisfy the following conditions fundamentally. 1. Choose a specific pixel and give required display information. a current can be passed for an OLED component through a 2.1-frame period -- although the transistor for switching is in liquid crystal as compared with the active-matrix method used for liquid crystal here, there is no transistor for a drive in the active matrix used for liquid crystal, and they are a sink and a transistor required in order to shine about a current at OLED. Although an ON state can be held because this reason impresses an electrical potential difference in the case of liquid crystal, in OLED, it is because it continues passing a current and a pixel is made into an ON state.
[0004] Therefore, by the OLED panel, the current source for continuing passing a current is required, and the transistor for a drive plays the role. First, if the scanning line is turned on, it will be accumulated in a capacitor C1 as a charge through the transistor T1 for switching. In order that this capacitor C1 may continue applying an electrical potential difference to the gate of the transistor T2 for a drive, even if the transistor T1 for switching becomes off, a current continues flowing through the transistor for a drive from a current supply source line, and a pixel can be turned on over an one-frame period. When displaying gradation using this configuration, it is necessary to impress the electrical potential difference according to gradation to the gate voltage of the transistor T2 for a drive. Here, if dispersion will be in the threshold electrical potential difference of T2 of the transistor for a drive of each pixel (it expresses also Vth hereafter) even if the same electrical potential difference is impressed to the gate electrode of the transistor T2 for a drive, the current value which flows for an OLED component by each pixel will change. Therefore, dispersion in the threshold electrical potential difference of the transistor for a drive will appear in a display as it is.
[0005] If the ON state current of a transistor is the transistor formed with the single crystal, it is very uniform, but with the low-temperature polycrystal transistor (it expresses also low-temperature poly-

Si TFT hereafter) which can be formed in a cheap glass substrate, since dispersion in the threshold has dispersion in the range exceeding **1.0V, ZARATSUKI by which the ON state current which flows the transistor T2 for a drive mixed nonuniformity, and a salt and pepper with dispersion and a display corresponding to this occurs. These poor display generates not only dispersion in a threshold electrical potential difference but dispersion in the mobility of TFT, dispersion of the OFF state current, and dispersion of parasitic capacitance. Therefore, in order to obtain a uniform display by the approach of displaying gradation in analog, it is necessary to control the property of a transistor strictly (V or less [For example, a threshold electrical potential difference **0.1]), and cannot be satisfied with the present low-temperature polycrystal poly-Si TFT of this spec. In order to solve this problem, various circuitry is proposed as shown in drawing 25 (B) - (D).

[0006] Drawing 25 (B) is SID98, DIGEST, and the circuit indicated by p.11. Four transistors are prepared in 1 pixel and it has the composition of making dispersion in the threshold electrical potential difference of the transistor T2 for a drive compensating by the capacitor, and acquiring a uniform current. However, although compensated, since the video signal (it expresses also data hereafter) is given on the electrical potential difference, as for the variation in the threshold electrical potential difference of the transistor T2 for a drive, no mobility other than the threshold voltage of the transistor for a drive etc. can compensate with this configuration variation in the parameter which gives ON current.

[0007] On the other hand, data were given with the current and the circuitry which compensates the property variation of the transistor T2 for a drive was proposed. Drawing 25 (C) is a configuration currently indicated by IEDM 98-p.875. Solution of the above-mentioned technical problem is aimed at by giving data with Current Idata.

[0008] However, since the current of which 1. program is done is programmed through an OLED component, when OLED has a big junction capacitance, this approach requires time amount for the write-in time amount of Idata, and cannot expect high-speed operation.

2. When a current path changes, the transistor for a drive (MN2) which controls a drive current to the switching transistor (MN4) connected to power-source Rhine serves as a source follower. Therefore, the source electrical potential difference of the transistor for a drive is changed with the property of the transistor for switching. It has which fault.

[0009] Moreover, the circuit of drawing 25 (D) is one of those can solve this. This circuit is indicated by **** technique ED2001-8SDM2001-8pp7. Since it becomes the configuration that the source electrode of the transistor for a drive (T3) is connected to Vdd, and the writing of Idata does not mind said OLED component, the charge to the junction capacitance of an OLED component is unnecessary, and serves as a circuit suitable for high-speed operation. Moreover, the circuit of drawing 25 (E) is raised as a modification. Actuation of the circuit of drawing 25 (E) is completely the same as circuit actuation and the essential target of drawing 24 (D).

[0010]

[Problem(s) to be Solved by the Invention] Here, in these circuits, after the transistor for sample hold (MNT1 [1]) for holding the transistor for signal current writing (MNT2 [3]) and gate voltage closes, if it is not made for neither the switch transistor for electrical-potential-difference supply (MN4) nor a current path changeover switch transistor (T four) to open, learn and there is nothing fundamentally, as indicated by IEDM98-pp875.

[0011] Moreover, on the other hand, it is driving in these circuits so that it may connect with the scanning line with the same transistor for sample hold (MNT1 [1]) for holding the transistor for signal current writing (MNT2 [3]), and gate voltage or ON/OFF may be carried out to coincidence. In the circuit of drawing 25 (C), when the same gate voltage is applied to the transistor for signal current writing (MN3), and the transistor for sample hold (MN1), since it surely becomes low, if those transistors have the same threshold property in the case of a p channel, MN1 will surely close previously the source potential and drain potential of MN1 from the source potential and drain potential of MN3.

[0012] Moreover, even if it closes to coincidence, and the threshold of MN1 becomes sufficiently lower than MN3 threshold and the transistor for current writing (MN3) and the switch transistor for electrical-potential-difference supply (MN4) close after MN3 If it closes before MN4 opens, since there will be no supply path of the electrical potential difference to the gate voltage of the transistor

for a drive (MN2) (the electrical potential difference from a cathode electrode is blocked by the OLED component), Since the electrical potential difference as the time of current writing with the almost same gate voltage of MN2 is held normally, it is satisfactory. Also in an n channel, it is [it becomes the same relatively] satisfactory although a polarity completely becomes reverse relation.
[0013] however, in the circuit of drawing 25 (D) and drawing 25 (E) It differs from the circuit of drawing 25 (C). Surely the source potential of the switch transistor for current writing (T2) or the potential of a drain electrode Rather than the source potential or drain potential of the transistor for sample hold (T1), since it becomes low by the threshold of the transistor for a drive (T3) (a part for -Vth [In the case of a p channel]) If it is made to operate with the same gate voltage, the direction of the switch transistor for current writing (T2) will surely close ahead of the transistor for sample hold (T1). If it does so, the recharge of the gate voltage of the transistor for a drive (T3) will be carried out until the transistor for sample hold (T1) closes toward power-source potential according to the potential of a signal line, and the current by which itself who is connected to the power source was programmed in the case of drawing 25 (E) in the case of drawing 25 (D). Therefore, the current (programmed) memorized at the time of writing changes by that cause, in the case of drawing 25 (D), increases and, in the case of drawing 25 (E), decreases.
[0014] Here, all that matters most is the case where this scan wave (gating waveform) has delay (wave ****). When it builds in a vertical-scanning circuit (gate circuit) by low-temperature polish recon especially, the amount of delay of a scan wave is large, and has dispersion. If the amount of delay is large, since the rate of increase or percentage reduction of a current by the recharge will become large according to it, if there is dispersion, it will generate dispersion in the current which flows to OLED. In this case, since it became current dispersion for every scanning line and the scan wave has extended horizontally in many cases, horizontal stripe-like unevenness is generated.
[0015] When the threshold of the switch transistor for current writing (T2) or the transistor for sample hold (T1) varies about 0.1V and between a contiguity pixel, in order to induce dispersion on the current which flows to OLED of a pixel and to make a display generate ZARATSUKI in the condition that there is delay of a scan wave, it stops moreover, almost generating the advantage of these circuits. In the display of an actual active-matrix mold, a problem becomes serious, so that it cannot say that there is no delay of a scan wave and becomes on a large scale and highly minute especially.
[0016] As opposed to the above-mentioned technical problem generated in the circuitry which it was possible for this invention to have solved the above-mentioned conventional trouble, and for the transistor which controls the current which flows to OLED to have not served as a source follower configuration, but to have made driver voltage low, and was suitable for high-speed operation Even if there is delay of a scan wave, it has a high margin to the variation and threshold variation of the amount of delay, and aims at offering the active-matrix mold OLED display which can acquire the good display engine performance without a stripe or ZARATSUKI, and high productivity, and its drive approach.
[0017]
[Means for Solving the Problem] In order to attain this purpose, the active-matrix mold OLED display and its drive approach of this invention have the following configurations and approaches.
[0018] In the display with which a unit pixel consists of two or more transistors and OLED components as the 1st configuration The 1st transistor by which the source electrode was connected to the power source into said unit pixel, The capacitor by which one electrode was connected to said power source, and the electrode of another side was connected to the gate electrode of said 1st transistor, Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. Another side of a source electrode or a drain electrode is connected to the gate electrode of said 1st transistor. Either the 2nd transistor and source electrode by which the gate electrode was connected to the 1st scanning line, or a drain electrode is connected to the drain electrode of said 1st transistor. The 3rd transistor by which another side of a source electrode or a drain electrode was connected to the signal line, and the gate electrode was connected to the 2nd scanning line, Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. The active-matrix mold OLED display characterized by having the 4th transistor by which another side of a source electrode or a drain electrode was connected to the OLED component, and the gate

electrode was connected to the 3rd scanning line is constituted.
[0019] In the display with which a unit pixel consists of two or more transistors and OLED components as the 2nd configuration The 1st transistor by which the source electrode was connected to the power source into said unit pixel, The capacitor by which one electrode was connected to said power source, and the electrode of another side was connected to the gate electrode of said 1st transistor, Either a source electrode or a drain electrode is connected to the gate electrode of said 1st transistor. The 3rd transistor by which either the 2nd transistor and source electrode by which the gate electrode was connected to the 1st scanning line, or the drain electrode was connected to the signal line, and the gate electrode was connected to the 2nd scanning line, Either the 4th transistor and source electrode by which either the source electrode or the drain electrode was connected to the OLED component, and the gate electrode was connected to the 3rd scanning line, or a drain electrode It connects with the drain electrode of said 1st transistor. Another side of a source electrode or a drain electrode Another side of the source electrode of said 2nd transistor, or a drain electrode, The active-matrix mold OLED display characterized by having the 5th transistor connected to another side of another side of the source electrode of said 3rd transistor or a drain electrode and the source electrode of said 4th transistor, or a drain electrode is constituted.
[0020] As the 3rd configuration, said 2nd and 3rd scanning lines are common, and the active-matrix mold OLED display by which it is being [it / the conductivity type with which said the 3rd transistor and 4th transistor differed from each other] characterized is constituted.
[0021] as the 4th configuration, said the 3rd transistor and said 4th transistor of another side are unjust, when one side is switch-on -- a connoisseur -- the active-matrix mold OLED display by which it is having-threshold property which will be in condition characterized is constituted.
[0022] As the 5th configuration, said transistor constitutes the active-matrix mold OLED display characterized by being the thin film transistor component which used polish recon.
[0023] As the 6th configuration, said 1st transistor constitutes the active-matrix mold OLED display characterized by being the transistor of a hole conductivity type.
[0024] As the 7th configuration, said 2nd transistor constitutes the active-matrix mold OLED display characterized by connecting to a serial two or more transistor components by which the gate electrode was connected to the common gate line, and changing.
[0025] As the 8th configuration, at least one of the transistor components used for the circuit for vertical scannings or level drive circuit of an active-matrix mold OLED indicating equipment As the 9th configuration which constitutes the active-matrix mold OLED display characterized by being formed in the transistor component and coincidence in a pixel, said vertical-scanning circuit The active-matrix mold OLED display characterized by including three different pulse width and the circuit which generates the scan wave which has a phase consists of one output of the shift register of the exterior or the interior.
[0026] As the 10th configuration, in some periods of a vertical-scanning period, said level drive circuit intercepts the current corresponding to said video signal, and constitutes the active-matrix mold OLED display characterized by having a charge circuit for making said signal line into fixed potential.
[0027] The active-matrix mold OLED display characterized by change of the luminescence brightness between said adjoining pixels being a maximum of 2% as the 11th configuration is constituted.
[0028] The display for personal digital assistants characterized by using the above-mentioned active-matrix mold OLED indicating equipment as the 12th configuration is constituted.
[0029] Large-sized television characterized by using the above-mentioned active-matrix mold OLED indicating equipment as the 13th configuration is constituted.
[0030] The highly minute monitor characterized by using the above-mentioned active-matrix mold OLED display as the 14th configuration is constituted.
[0031] In the display with which a unit pixel consists of two or more transistors and OLED components as the 1st approach By activating the 1st scanning line and 2nd scanning line, the 1st gate electrode and drain electrode of a transistor After making it switch-on through the 2nd transistor, letting said the 1st transistor and 3rd transistor pass and passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st

scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], After making said 2nd scanning line inactive and making said 2nd scanning line inactive, the 3rd scanning line is activated, it lets the 4th transistor pass, and the current of the value corresponding to said video signal is passed to said OLED.

[0032] In the display with which a unit pixel consists of two or more transistors and OLED components as the 2nd approach While activating the 1st scanning line and 2nd scanning line and making the 1st gate electrode and drain electrode of a transistor into switch-on through the 2nd transistor Impress predetermined bias voltage to the gate voltage of the 5th transistor, and it lets said 1st transistor, the 3rd transistor, and the 5th transistor pass. After passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], After making said 2nd scanning line inactive and making said 2nd scanning line inactive, the 3rd scanning line is activated, it lets the 4th transistor pass, and the current of the value corresponding to said video signal is passed to said OLED.

[0033] In the display with which a unit pixel consists of two or more transistors and OLED components as the 3rd approach By activating the 1st scanning line and 2nd scanning line, the 1st gate electrode and drain electrode of a transistor After making it switch-on through the 2nd transistor, letting said the 1st transistor and 3rd transistor pass and passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], Said 2nd scanning line is activated to inactive and the 4th transistor to the 3rd transistor, it lets the 4th transistor pass, and the current of the value corresponding to said video signal is passed to said OLED.

[0034] In the display with which a unit pixel consists of two or more transistors and OLED components as the 4th approach While activating the 1st scanning line and 2nd scanning line and making the 1st gate electrode and drain electrode of a transistor into switch-on through the 2nd transistor Impress predetermined bias voltage to the gate voltage of the 5th transistor, and it lets said 1st transistor, the 3rd transistor, and the 5th transistor pass. After passing the current of the value corresponding to a video signal towards a signal line from a power source, by making the 1st scanning line inactive After holding the gate voltage of said 1st transistor and carrying out inactive [of said 1st scanning line], Said 2nd scanning line is activated to inactive and the 4th transistor to the 3rd transistor, it lets the 4th transistor pass, and the current of the value corresponding to said video signal is passed to said OLED.

[0035] In the display with which a unit pixel consists of two or more transistors and OLED components as the 5th approach Either a source electrode or a drain electrode is connected to the gate electrode of the 1st transistor by which the source electrode was connected to the power source. The electrical potential difference of the 1st scanning line connected to the gate electrode of the 2nd transistor by which another side of a source electrode or a drain electrode was connected to the drain electrode of said 1st transistor said 2nd transistor is unjust -- a connoisseur, after making it inactive so that it may be in a condition Either a source electrode or a drain electrode is connected to the drain electrode of the 1st transistor. The electrical potential difference of the 2nd scanning line with which it connected with the signal line and another side of a source electrode or a drain electrode was connected to the gate electrode of the 3rd transistor It is made inactive. said 3rd transistor is unjust -- a connoisseur -- so that it may be in a condition Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. The electrical potential difference of the 3rd scanning line with which another side of a source electrode or a drain electrode was connected to the gate electrode of the 4th transistor connected to the OLED component is activated as [be / in switch-on / said 4th transistor component].

[0036] In the display with which a unit pixel consists of two or more transistors and OLED components as the 6th approach Either a source electrode or a drain electrode is connected to the gate electrode of the 1st transistor by which the source electrode was connected to the power source. The electrical potential difference of the 1st scanning line connected to the gate electrode of the 2nd transistor by which another side of a source electrode or a drain electrode was connected to the drain electrode of said 1st transistor said 2nd transistor is unjust -- a connoisseur, after making it inactive

so that it may be in a condition Either a source electrode or a drain electrode is connected to the drain electrode of the 1st transistor, and another side of a source electrode or a drain electrode is connected to a signal line. The gate electrode of the 3rd transistor, Either a source electrode or a drain electrode is connected to the drain electrode of said 1st transistor. in the electrical potential difference of the 2nd scanning line with which another side of a source electrode or a drain electrode was connected to the gate electrode of the 4th transistor connected to the OLED component, said 3rd transistor is unjust -- a connoisseur -- it will be in a condition and will be made for said 4th transistor component to be in switch-on

[0037] In the display which consists of the above-mentioned OLED component as the 7th approach either a source electrode or a drain electrode It connects with the drain electrode of said 1st transistor. Another side of a source electrode or a drain electrode Another side of the source electrode of said 2nd transistor, or a drain electrode, Predetermined bias voltage is impressed to the gate electrode of the 5th transistor connected to another side of another side of the source electrode of said 3rd transistor, or a drain electrode and the source electrode of said 4th transistor, or a drain electrode.

[0038] As the 8th approach, the 1st transistor and 5th transistor set up said both predetermined bias voltage so that it may operate in a saturation region.

[0039]

[Embodiment of the Invention] (Gestalt 1 of implementation of invention) The circuitry of this invention is shown in drawing 1 . By being formed of two or more transistors and OLED components which a unit pixel becomes from at least four, and activating the 1st scanning line GL1 While the 2nd transistor MSH opens so that between the gate of the 1st transistor MDR and a drain may be short-circuited It lets the 1st Transistor MDR and 3rd transistor MWR pass by activating the 2nd scanning line GL2. The current of the value corresponding to a video signal to the capacitor CS connected between a sink, and the gate of the 1st transistor MDR and the source After remembering that the gate voltage of the 1st transistor MDR passes the signal current After making the 1st scanning line GL1 inactive and making the 2nd transistor MSH into an OFF state, The 2nd scanning line GL2 is made inactive, the 3rd transistor MWR is made into an OFF state, the 3rd scanning line GL3 is activated after that, and a pixel circuit is constituted so that said current may be passed for the 4th Transistor MCH and OLED component.

[0040] This circuit has four transistors in 1 pixel, the source of the 1st transistor MDR is connected to a power-source line (voltage source), the gate of MDR is connected to the source of the 2nd transistor MSH, the gate of the 2nd transistor MSH is connected to the 1st scanning line GL1, and the drain of MSH is connected to the source of the drain of MDR, and the 3rd transistor MWR, and the source of the 4th transistor MCH. Moreover, the drain of MWR is connected to a signal line DATA, the gate is connected to the 2nd scanning line GL2, the gate of MCH is connected to the 3rd scanning line GL3, and the drain is connected to the anode electrode of OLED.

[0041] Hereafter, the means and operation are explained.

[0042] The drive approach (timing chart) of the pixel of this invention and drawing 3 show the equal circuit of the pixel in the 2nd timing (t1-t2) of the conventional pixel to the drive approach (timing chart) of the conventional pixel, and drawing 4 at drawing 2 , and the representative circuit schematic in each timing of the pixel of this invention and drawing 5 show change of the operating point of the drive transistor MDR of this invention and the conventional pixel to drawing 6 .

[0043] The drive circuit of this invention is controlled by three timing. The first period is timing (-t1) which makes a required current value memorize. When MWR and MSH open to this timing, it is set to drawing 3 A as an equal circuit. Here, MDR will be in the diode connection condition made into the condition that the gate and a drain were connected, and, thereby, the predetermined current ISIG corresponding to a video signal will flow from a signal line through this MDR and MWR. At this time, a current I2 flows also to MSH, and if the gate voltage of MDR flows until it reaches the gate voltage V1 which passes I1=ISIG, and it amounts to V1, a current I2 will not flow.

[0044] The second timing is MSH and closed timing (t1-t2). The equal circuit at that time is set to drawing 3 B. Thereby, Current ISIG is separated from a voltage source and a current source, while the gate voltage of MDR had maintained V1, flowing to MWR. The 3rd timing (t2-) is timing which closes MWR and opens MCH. The equal circuit at that time serves as drawing 3 C. At this time, the

timing which opens coincidence or MCH carries out timing which MWR closes, and timing which MCH opens after the timing which closes MWR. Thereby, the current value ISIG memorized by MDR flows into OLED through MCH. the predetermined current ISIG corresponding to [although the operating point of MDR moves to V2 of drawing 6 , in order that the transistor of MDR may operate in a saturation region, the current value of MDR before and behind a change does not change fundamentally, and] a video signal -- ' (**ISIG) -- it flows to OLED.

[0045] On the other hand, in the conventional pixel, since the scanning lines GL1 and GL2 are common, the scan wave of MSH and MWR becomes the same. Since the source potential of MSH or the potential of a drain electrode surely becomes low rather than the source potential or drain potential of MWR by the threshold of MDR (a part for -Vth [In the case of a p channel]) at this time, if it is made to operate with the same gate voltage, the direction of MWR will close ahead of MSH. The equal circuit at that time serves as drawing 5 . If it does so, the recharge of the gate voltage of MDR will be carried out until MSH closes completely toward power-source potential according to the current by which itself who is connected to the power source was programmed. Therefore, the current (programmed) ISIG memorized at the time of writing changes by that cause, and decreases depending on a time delay. as the operating point of MDR at this time having been shown in drawing 6 -- the 2nd timing -- gate voltage -- V1 to V1 -- ' -- decreasing -- the 3rd timing -- V2 from V1' -- ' -- changing -- ISIG -- ISIG -- " -- it changes and a large electrical-potential-difference change occurs.

[0046] Although all four transistors to produce could be transistors of the same P channel mold or an N channel mold and could be transistors of a different mold, they were altogether used as the transistor of a P channel with the gestalt of this operation. Moreover, with the gestalt of this operation, the thin film transistor (it is also called TFT) of low-temperature polish recon was used for the transistor. However, a transistor may not be what was restricted to the thin film transistor of low-temperature polish recon, and the transistor of the elevated-temperature polish recon which may use the single crystal transistor on a silicon wafer, and is created on continuation grain boundary silicon (CGS) or a quartz substrate is sufficient as it.

[0047] Moreover, although TFT of the planar mold of the top gate was used for the cross-section structure of a transistor with the gestalt of this operation, the bottom gate is sufficient as it, and a stagger mold or a reverse stagger mold is sufficient as it. Furthermore, that in which the impurity range (the source, drain) was formed using the self aryne method may also be depended on a non-self aryne method, and these are the criteria of this invention at all.

[0048] The flat-surface configuration of the pixel of the gestalt of this operation is shown in drawing 7 . On a substrate, the wiring electrode group for supplying an electrical potential difference and a current to the pixel arranged in the shape of a matrix is prepared. The signal line DATA in drawing 7 is wiring for telling a video-signal current, the scanning lines GL1-GL3 are wiring for telling the control signal for making the transistor of a pixel actively/inactive, and a power-source line is wiring for supplying an anode electrical potential difference to the hole impregnation electrode 31 (a pixel electrode, anode). Each wiring electrode has the desirable one where resistance is lower, and it is used for the wiring electrode for the metal containing any one sort, such as aluminum, Ti or titanium nitride (TiN), and Ta, Mo, Cr, W, Cu, Nd, Zr, or two sorts or more, making it into the laminated structure more than a monolayer or two-layer. However, in this invention, it is not restricted to this ingredient.

[0049] Moreover, the capacitor CS holding the gate voltage of the 1st transistor MDR is formed in general in the non-display field between the adjoining pixels. When creating a full color panel by low-molecular OLED, in order to form an OLED layer by the mask vacuum evaporationo with a metal mask, the width of face of the non-display field between the adjoining pixels is set to about 10-20 micrometers. Since this part turns into a part which does not contribute to luminescence, in the case of the method which takes out light from a glass substrate [in which the transistor was formed] side, it becomes an effective means for the improvement in a numerical aperture to form the maintenance capacitor CS in this field. The structure of an OLED component is described below.

[0050] The example of a configuration of the OLED display of the gestalt of this operation is shown in drawing 8 . With the gestalt of this operation, since the method (bottom drawing is called hereafter) which takes out light from a glass substrate [in which the transistor was formed] side was

used, ITO which is a transparent electrode was used for the hole impregnation electrode 31.
[0051] First, the array of a transistor is formed on a substrate at a desired configuration. And by the spatter, membranes are formed and patterning of the ITO which is a transparent electrode as a pixel electrode on the flattening film is carried out. Then, the laminating of an OLED layer, the electron injection electrode, etc. is carried out.
[0052] The laminating of the OLED structure 11 which has ITO31 from which the OLED indicating equipment shown in drawing 8 serves as the hole impregnation electrode 31 through an insulating layer 38 with the array of a thin film transistor TFT on a glass substrate 35, and an organic layer 22 and the electron injection electrode 32 is carried out. Since outgoing radiation of the light needs to be carried out from the direction of a rear face of a substrate as a substrate ingredient, the transparence thru/or translucent ingredient of glass, a quartz, resin, etc. can be used.
[0053] What is necessary is just to usually set it to about 100-1000nm as thickness of the whole which combined the hole impregnation electrode 31 and the wiring electrode of TFT used as the substrate of the OLED structure 11, although there is especially no limit.
[0054] The insulating layer 38 prepared between the wiring electrode of TFT and the organic layer of the OLED structure 11 What formed inorganic system ingredients, such as silicon oxide of SiO2 grade, and silicon nitride, with a spatter or vacuum deposition, As long as the paint film of resin system ingredients, such as a silicon oxide layer formed by SOG (spin-on glass), a photoresist, polyimide, and acrylic resin, etc. has insulation, it may be any, but since the thicker evener one is good, the organic film is more desirable. Moreover, as for the hygroscopic organic high film, it is desirable [an insulating layer 38] to make it the structure where the open air cannot be touched in order to protect the weak OLED component 11 for moisture.
[0055] As the technique of colorization, it realized with the gestalt of this operation by distinguishing three kinds of ingredients with a differing-, respectively luminescence peak (R, G, B) with a metal mask. Moreover, there is also a method of there being also the approach of acquiring with the combination of the OLED structure of white luminescence for example, and the color filter of RGB as an option, and obtaining three colors of RGB from the OLED structure of blue luminescence by the wavelength conversion layer.
[0056] Next, the OLED structure 11 which constitutes the OLED display of this invention is explained. The OLED structure 11 of this invention has the hole impregnation electrode 31 which is a transparent electrode, one or more sorts of organic layers 22, and the electron injection electrode 32. An organic layer has at least one-layer hole transportation layer and a luminous layer, respectively, for example, has an electron injection transportation layer, a luminous layer, a hole transportation layer, and a hole impregnation layer one by one. In addition, there may not be a hole transportation layer. The organic layer of the OLED structure 11 of this invention can be considered as various configurations, and electron injection and a transportation layer may be omitted, it may consider as a luminous layer and one, or it may mix a hole impregnation transportation layer and a luminous layer. An electron injection electrode consists of the small metal, compound, or alloys of the work function preferably formed with vacuum deposition, such as vacuum evaporationo and a spatter.
[0057] They are ITO (tin dope indium oxide), IZO (zinc dope indium oxide), ZnO and SnO2 since it is the structure which takes out the light which emitted light from the hole impregnation electrode 31 side as a hole impregnation electrode 31, and In 2O3. Especially ITOIZO is desirable although the ingredient of transparency etc. is mentioned. As for the thickness of the hole impregnation electrode 31, it is [that what is necessary is just to have the thickness more than / which can perform hole impregnation enough / fixed] usually desirable to be referred to as about 10-500nm. Moreover, the thinner one of these film is desirable in the range which does not spoil a permeability property in order to prevent a short circuit with the cathode in an edge. When actually using it, the cross protection by reflection by hole impregnation electrode 31 interfaces, such as ITO, should just set up the thickness and the optical constant of an electrode so that optical ejection effectiveness and color purity may fully be satisfied. Although the hole impregnation electrode 31 can be formed with vacuum deposition etc., forming by the spatter is desirable. What is necessary is not to restrict and just to use inert gas, such as Ar, helium, Ne, Kr, and Xe, or these mixed gas especially as sputtering gas.

[0058] The electron injection electrode 32 consists of the small metal, compound, or alloys of the work function preferably formed with vacuum deposition, such as vacuum evaporationo and a spatter. In order to raise metallic element simple substances, such as K, Li, Na, Mg, La, Ce, calcium, Sr, Ba, aluminum, Ag, In, Sn, Zn, and Zr, or stability as a component of the electron injection electrode formed, it is desirable to use the alloy system containing them of two components and three components. As an alloy system, Ag-Mg (Ag:1 - 20at%), aluminum-Li (Li:0.3 - 14at%), In-Mg (Mg:50 - 80at%), aluminum-calcium (calcium:5 - 20at%), etc. are desirable, for example.
[0059] What is necessary is just to set preferably 0.1nm or more of thickness of an electron injection electrode thin film to 1nm or more that what is necessary is just to consider as the thickness more than [which can perform electron injection enough] fixed.
[0060] A hole impregnation layer has the function which makes easy impregnation of the hole from the hole impregnation electrode 31, and a hole transportation layer has the function which bars the function and electron which convey a hole, and is also called a charge impregnation layer and a charge transportation layer.
[0061] An electron injection transportation layer is prepared when the electron injection transportation function of the compound used for a luminous layer is not so high, and it has the function which bars the function which makes easy impregnation of the electron from an electron injection electrode, the function to convey an electron, and a hole.
[0062] A hole impregnation layer, a hole transportation layer, and an electron injection transportation layer increase - Make the hole and electron which are poured in to a luminous layer shut up, make a recombination field optimize, and improve luminous efficiency.
[0063] In addition, an electron injection transportation layer may be separately prepared in a layer with an impregnation function, and a layer with a transportation function.
[0064] Although the thickness of a luminous layer, the thickness which combined the hole impregnation layer and the hole transportation layer, and especially the thickness of an electron injection transportation layer are not limited but it changes also with formation approaches, it is usually desirable to be referred to as about 5-100nm.
[0065] What is necessary is just to make them into comparable as the thickness of a luminous layer or 1 / about 10 to 10 times, although the thickness of a hole impregnation layer and a hole transportation layer and the thickness of an electron injection transportation layer are based on the design of recombination / luminescence field. As for an impregnation layer, it is [each thickness in the case of dividing the thickness of a hole impregnation layer and a hole transportation layer, and an electronic injection layer and an electronic transportation layer] desirable to set 1nm or more and a transportation layer to 20nm or more. The upper limit of the thickness of the impregnation layer at this time and a transportation layer is usually about 100nm in an impregnation layer in about 100nm and a transportation layer. It is also the same as when preparing two layers of impregnation transportation layers about such thickness. Moreover, taking into consideration the carrier mobility and the carrier consistency (decided by ionization potential and the electron affinity) of the luminous layer and electron injection transportation layer to combine, or a hole impregnation transportation layer, by controlling thickness, it is possible to design a recombination field and a luminescence field freely, and design of the luminescent color, control of the luminescence brightness and emission spectrum by the cross protection of two electrodes, and control of the spatial distribution of luminescence are enabled.
[0066] The luminous layer of the OLED component of this invention is made to contain the fluorescence matter which is the compound which has a luminescence function. Bluish green color luminescent material which is indicated by metal complex coloring matter, such as tris (8-quinolinolato) aluminum [Alq3] which is indicated by JP,63-264692,A etc., JP,6-110569,A (phenyl anthracene derivative), a 6-114456 official report (tetra-aryl ethene derivative), JP,6-100857,A, this JP,2-247278,A, etc. as this fluorescence matter, for example is mentioned.
[0067] Moreover, the various organic compounds indicated by JP,63-295695,A, JP,2-191694,A, JP,3-792,A, JP,5-234681,A, JP,5-239455,A, JP,5-299174,A, JP,7-126225,A, JP,7-126226,A, JP,8-100172,A, and EP0650955A1 grade can be used for a hole impregnation layer and a hole transportation layer. It is desirable to use a vacuum deposition method for formation of a hole impregnation transportation layer, a luminous layer, and an electron injection transportation layer,

since a homogeneous thin film can be formed.
[0068] Furthermore, it closes with a sealing agent 40 so that moisture may not go into an OLED layer. With the gestalt of this operation, although the laminated structure of a metal thin film and the organic film is used, the approach of making glass rivaling using a sealant may be used.
[0069] Thus, direct current voltage was impressed to the produced OLED display, and the continuation drive was carried out with the fixed current density of 10 mA/cm2. As for the OLED structure, 5.0V, 100 cd/cm2, and a color coordinate have checked luminescence of the white of x= 0.30 and y= 0.33. A blue light-emitting part is brightness 100 cd/cm2. For a color coordinate, x= 0.129, y= 0.105, and a green light-emitting part are brightness 200 cd/cm2. For a color coordinate, x= 0.340, y= 0.625, and a red light-emitting part are brightness 125 cd/cm2. The color coordinate was acquired for the luminescent color of x= 0.649 and y= 0.338.
[0070] The effectiveness of the gestalt of this operation is shown below. Drawing 9 shows change of the OLED current IOLED over the time delay of a scan wave (gating waveform). the case where drawing 9 A does not have dispersion in the threshold VTH of a transistor, and the threshold of MSH -0.1V -- the case where drawing 9 B does not have dispersion in the threshold VTH of a transistor in the gating waveform time delay dependency of the OLED current IOLED in the case of being low, and the threshold of MSH -0.1V -- the variation (%) of the OLED current IOLED in the case of being low is shown. As shown in drawing 9 , since an OLED current changed sharply depending on the time delay of a gating waveform and in the case of this invention was hardly dependent on a time delay although the horizontal stripe by dispersion in the amount of delay occurs, by the conventional pixel, it was completely lost by generating of a horizontal stripe.
[0071] Moreover, change of an OLED current when the threshold of each four transistor components changes to drawing 10 is shown. Drawing 10 A and B is the conventional pixels, in drawing 10 C and D, in ISIG=1microA, in ISIG=0.01microA, B of A is the pixel of this invention, and, as for C, in ISIG=1microA, D shows the case of ISIG=0.01microA. By the conventional pixel, as shown in drawing 10 A and B, if there is change of the threshold of MSH and MWR, it will be intense and an OLED current will change, but as shown in drawing 10 C and D, even if they change in the case of this invention, an OLED current hardly changes but is stable.
[0072] Thereby, although the conventional pixel is **0.1V, it was able to be set to **0.8V and was able to be made to expand sharply in the gestalt of this operation on the conditions on which for example, current dispersion permits the variation margin of the threshold electrical potential difference of each transistor to **2%. Moreover, in the conventional pixel, to MSH and MWR having carried out the ** rule, the pixel of this invention was able to become the form by which a ** rule is carried out to threshold dispersion of the drive transistor MDR of current program method original, and was able to have the very large threshold variation margin.
[0073] As mentioned above, the condition that there is delay of a scan wave and the amount of delay differs in the gestalt of this operation, Since the current which flows to OLED of a pixel also in the condition that the threshold of the switch transistor MWR for current writing or the transistor MSH for sample hold varies between contiguity pixels does not have dispersion, It has a high margin to the variation and threshold variation of the amount of delay. It has the good display engine performance without a stripe or ZARATSUKI, the linearity of an OLED current to the signal current is high, consequently the yield is high, and a large size and a highly minute OLED display panel with sufficient productivity can be obtained.
(Gestalt 2 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.
[0074] With the gestalt of this operation, as shown in drawing 11 , the cascade transistor MCS is connected to MDR. although it is satisfactory if it is the saturation area property of an ideal transistor in case the operating point of MDR moves to V2 from V1 with the gestalt 1 of operation, it is shown in drawing 12 -- as -- an Early condenser or a gate length modulation, and a thing further called the kink effectiveness -- ISIG -- a drain electrical potential difference -- following -- ISIG -- ' -- it is made to go up Thereby, if there is variation deltaVth of the threshold of MDR, it will serve as variation in the OLED current IOLED, and will appear. Therefore, it is before and after the change of MWR and MCH, and these operations must be reduced in order to stabilize Current ISIG.
[0075] therefore, the thing for which at least five transistors are constituted, cascade connection of

the transistor MCS is carried out to MDR as shown in drawing 11 , and bias voltage is made suitable -- drawing 12 -- becoming a property [like], the change by the operating point of Current ISIG becomes very small. At this time, both the range where bias voltage is suitable means the conditions on which MDR and MCS operate in a saturation region.

[0076] In addition to the effectiveness of the gestalt 1 of operation, with the gestalt of this operation, the margin of the threshold variation of MDR was able to be sharply raised from **0.8V to **2V.

(Gestalt 3 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.

[0077] With the gestalt of this operation, the 2nd and the 3rd scanning line were made common by having differed the conductivity type of the 3rd transistor and the 4th transistor. The configuration of the pixel circuit of the gestalt of this operation is shown in drawing 13 . With the gestalt of this operation, the transistor of n channels (it is also called an electronic conduction mold) and the 4th transistor MCH were used as the transistor of p channels (it is also called a hole conduction mold) for the 3rd transistor MWR. Since another side will be in an OFF condition when one side is in ON condition even if MWR and MCH are connected to the common transistor by this, an approach to change the current of this invention is not spoiled.

[0078] In addition to the effectiveness of the gestalt 1 of operation, with the gestalt of this operation, the numerical aperture of the improvement in a yield by simplification of a drive circuit and a pixel can be raised by reducing the number of scanning lines.

(Gestalt 4 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation, and the gestalt 3 of operation except for the following.

[0079] With the gestalt of this operation, if the path for which a current flows has branching in case it moves from the 2nd timing to the 3rd timing like the gestalt 1 of operation as fundamental timing of operation in addition to the configuration of the gestalt 3 of operation, the drain current of MDR increases, and it cannot memorize to the gate voltage of MDR so that the current value corresponding to a video signal may be passed. After MWR surely turned off to the timing from which the scanning line changes by controlling each other threshold, it was made for MCH to turn on with the gestalt of this operation, when MWR and MCH are made into a different electric conduction form like the gestalt 3 of operation. Specifically, the threshold of 2**2V and the 4th transistor MWR (p channels) was set to -2**2V for the threshold of the 3rd transistor MSH (n channels). An approach to change the current of this invention is not spoiled without two transistors being in ON condition at coincidence, even if this applies the same scan voltage waveform.

[0080] With the gestalt of this operation, the numerical aperture of the improvement in a yield by simplification of a drive circuit and a pixel can be raised by reducing the number of scanning lines like the gestalt 3 of operation.

(Gestalt 5 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.

[0081] MDR is constituted from a gestalt of this operation by the p channel mold polish recon thin film transistor. Thereby, the kink effectiveness shown in drawing 6 can be reduced rather than the case where n channel mold polish recon is used.

[0082] Thereby, although the margin of the threshold variation of MDR was about **0.3V, when it was a p channel mold polish recon thin film transistor in the case of n channel mold polish recon, it was able to be made to improve sharply to **0.8V.

(Gestalt 6 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.

[0083] The transistor which constitutes an active matrix is constituted from a gestalt of this operation by the p channel mold polish recon thin film transistor, and it was made the multi-gate structure where MSH was more than the dual gate. In order that MSH may act as a switch for electrical-potential-difference maintenance of the gate voltage of MDR, the property that an ON/OFF ratio is high as much as possible is required. The leak current value in various gate structures is shown in drawing 14 . From this, the structure of the gate is understood that the multi-gate structure beyond dual gate structure is required.

[0084] Thereby, the occupancy area of the maintenance capacitor CS could be reduced and the numerical aperture was able to be made to improve 5 point with the gestalt of this operation in

addition to the effectiveness of the gestalt 1 of operation.
(Gestalt 7 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.
[0085] The transistor which constitutes an active matrix was constituted from a gestalt of this operation by the polish recon thin film transistor, and while creating the transistor which constitutes a pixel for the precharge circuit set as the vertical-scanning circuit and signal line of an active-matrix OLED indicating equipment on a predetermined electrical potential difference before current writing, it really formed on the substrate.
[0086] The external view of the whole active-matrix OLED display is shown in drawing 15 . At least four or more transistors are required for this invention in a unit pixel. Therefore, it is suitable to use polish recon with high mobility as an ingredient of an active component as an ingredient of the transistor which constitutes these. Therefore, the circumference circuit which drives this panel is also doubled and it becomes possible to really form. Moreover, although the vertical-scanning circuit and the precharge circuit were built in, when built-in of a signal side circuit also uses a single crystal transistor as a gestalt of this operation as a circuit to build in, it can do easily. These considered the engine performance of a transistor, with the gestalt of this operation which should just determine the class of circuit to build in, could use the surrounding frame field as the compact, and were able to lightweight-ize the whole panel while in addition to the effectiveness of the gestalt 1 of operation the number of nodes with an external circuit could be reduced and mechanical dependability went up by building in a circumference circuit.
(Gestalt 8 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation, and the gestalt 7 of operation except for the following.
[0087] With the gestalt of this operation, it formed on the glass substrate, using polish recon as a circuit which generates the scan wave which has one output to three different pulse width and phases of a shift register for the vertical-scanning circuit of the gestalt 3 of operation. The circuit diagram of the vertical-scanning circuit of the gestalt of this operation is shown in drawing 18 from drawing 16 . Vertical-scanning wave phi1 to phi 3 of three specifications with different pulse width as shown in drawing 2 of the gestalt 1 of operation, and a phase can be generated by inputting the output INB of one shift register into one side of three NOR circuits, and controlling it by the three control lines OEVA, OEVB, and OEVC on another side.
[0088] In addition to the effectiveness of the gestalt 1 of operation, and the gestalt 7 of operation, compared with the case where three steps of shift registers are constituted independently, respectively, the scan wave which has three different pulse width and phases can be generated, and surrounding narrow picture frame-ization can be attained by very little circuitry with the gestalt of this operation.
(Gestalt 9 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation, and the gestalt 7 of operation except for the following.
[0089] While forming the transistor of the pixel of the gestalt 1 of operation, with the gestalt of this operation, in some periods of a vertical-scanning period, the current corresponding to a video signal was intercepted and the charge circuit (a precharge circuit is called hereafter) for making a signal line into fixed potential was formed on the glass substrate using polish recon. The circuit diagram of precharge of the gestalt of this operation is shown in drawing 19 .
[0090] Thereby, with the gestalt of this operation, in addition to the effectiveness of the gestalt 1 of operation, and the gestalt 7 of operation, the float of black level or length which poses a problem in the pixel circuit of the gestalt of this operation of a current write-in method has been improved, and improvement in a contrast ratio was able to be aimed at.
(Gestalt 10 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.
[0091] With the gestalt of this operation, the amount of fluctuation of brightness (the amount of currents) makes it to less than 2%. Axis-of-abscissa brightness is shown in drawing 20 , and the amount of fluctuation (deltaI-I) of brightness (Bcd/m2) is shown on an axis of ordinate. If the amount of fluctuation has 2% or more of brightness in the brightness field to 1-cd/m2 to 1000 cd/m2, human being will recognize the changed boundary line. Therefore, it is required for the amount of fluctuation of brightness (the amount of currents) to be less than 2%.

[0092] In the OLED display of this invention, when there was a V **0.8 [more than] difference of threshold ****** of MDR of an adjacent pixel, it turned out that the middle luminescent spot which becomes the origin of ZARATSUKI comes. Therefore, in order to suppress fluctuation of brightness within 2%, when the difference of threshold ****** of MDR of an adjacent pixel considers as less than [**0.8V], brightness variation of a contiguity pixel is made to below ******.
[0093] Moreover, the current value Ids in the saturation region of the 1st transistor is formula Ids=kx (Vgs-Vth) 2 (1+ Vds*lambda) the bottom.
If lambda of the above-mentioned formula has fluctuation even when fluctuation of a threshold does not exist even if between the pixels which come out, and adjoin when expressed, the current value which flows OLED will be changed. The result of having carried out simulation of the current value by fluctuation of lambda to the axis of abscissa lambda and the axis of ordinate is shown in drawing 21 . In order to suppress fluctuation within **2%, lambda must be held down to 0.05 or less.
[0094] Furthermore, when the grain boundaries of the crystal included in a channel by setting channel length to 15 micrometers or more increase in number showed that it was possible for electric field to be eased, and for the kink effectiveness to be suppressed low, and to hold down the value of lambda or less to 0.05. This is for the rate of fluctuation of the effective channel length by the drain electrical potential difference to decrease, when L is lengthened. The simulation result is shown in drawing 22 .
[0095] furthermore, the case where it considers as the minimum value Ioff of the OFF state current of the capacitor Cs for maintenance, and the 3rd transistor MSH -- a degree type -- Cs/Ioff>0.2 (F/A)

******** -- it becomes like. The simulation result of the current value which flows the OFF state current of MSH on an axis of abscissa, and flows OLED on an axis of ordinate at drawing 23 is shown. By setting the OFF state current of MSH to 5 or less pAs shows that it is possible to stop the current value change which flows OLED to 2% or less. This is because the charge stored between the GETO sources of MDR (both ends of a capacitor) in the electrical-potential-difference condition of not writing in cannot be held between 1 fields, when leakage current increases. Therefore, if the capacitor Cs for maintenance is large, the permissible dose of the OFF state current will also become large. We found out that fluctuation of the current value between contiguity pixels could be suppressed to 2% or less by filling said formula.
[0096] Furthermore, 50-micrometer 2 or less and the capacitor CS for maintenance are set to 0.5pF or more for the channel width (W) x channel length (L) of MSH. In the above-mentioned drive approach, the electrical potential difference between the sow sault gates of the transistor of M1 receives fluctuation with the parasitic capacitance of MSH, in case MSH changes from ON to an OFF state. When MSH becomes off from ON, amount of fluctuation deltaVoff of the electrical potential difference by this is expressed with a degree type.
deltaVoff=Con/(Cs+Con)x(Von-Vth)+Coff/(Cs+Coff)x(Vth-Voff)
Con and Voff are [the threshold voltage of MSH and Cs of the capacity of ON of MSH and the transistor in an OFF state and Vth] the values of storage capacitance here. Therefore, deltaVoff is influenced of the variation in threshold voltage. In order to make this effect small, there is the need of making size of MSH small and making the value of deltaVoff small.
[0097] L*W of MSH was found [50 micrometer2 or less and CS] by that it must be referred to as 0.5pF or more in order to have suppressed fluctuation of the current value between contiguity pixels to 2% or less.
(Gestalt 11 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.
[0098] With the gestalt of this operation, the active-matrix mold OLED indicating equipment of this invention was used for the display for personal digital assistants.
[0099] Thereby, the good display of a compact and display quality is realizable. This property is in agreement with the engine performance for which the display for personal digital assistants is asked.
(Gestalt 12 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.
[0100] With the gestalt of this operation, the active-matrix mold OLED indicating equipment of this invention was used for the high definition large-sized display. Also in the high definition large,

large-sized display of wave delay, the good display of display quality is realizable because it is with the OLED component of this invention.
(Gestalt 13 of implementation of invention) The gestalt of this operation is the same configuration as the gestalt 1 of operation except for the following.
[0101] With the gestalt of this operation, the array of TFT is first formed on a substrate at a desired configuration. And by the spatter, membranes are formed and patterning of Ag which is an electrode opaque as a pixel electrode on the flattening film is carried out. Then, the laminating of an OLED layer, the electron injection electrode, etc. is carried out. The example of a configuration of the OLED display of this invention is shown in drawing 24 . The laminating of the OLED structure which has MgAg34 used as the metal membrane 33 from which the OLED indicating equipment shown in drawing 24 serves as the hole impregnation electrode 31 through an insulating layer 38 with the array of a thin film transistor TFT on a glass substrate 11, and an organic layer 22 and an electron injection electrode is carried out. As shown in drawing 24 , although the metaled reflection factor of the hole impregnation electrode 31 is high, in the case of the method (upper drawing is called hereafter) which takes out light from the opposite side, luminous efficiency of direction improves the transistor side of an OLED component.
[0102] Since outgoing radiation of the light is carried out from the direction of a front face of a substrate as a substrate ingredient, in addition to the transparence thru/or translucent ingredient of glass, a quartz, resin, etc., nontransparent ingredients, such as stainless steel, can also be used. Moreover, since the sealing agent 40 needed to make the ejection side transparence, the laminated structure of only the organic film was used for it so that moisture might not go into an OLED layer.
[0103] As compared with the gestalt 1 of operation with the gestalt of this operation, the conditions of a luminous layer ingredient etc. are fundamentally the same.
[0104] Thus, direct current voltage was impressed to the produced OLED display, and the continuation drive was carried out with the fixed current density of 10 mA/cm2. As for the OLED structure, 5.0V, 150 cd/cm2, and a color coordinate have checked luminescence of the white of x= 0.30 and y= 0.33. A blue light-emitting part is brightness 150 cd/cm2. For a color coordinate, x= 0.129, y= 0.105, and a green light-emitting part are brightness 300 cd/cm2. For a color coordinate, x= 0.340, y= 0.625, and a red light-emitting part are 2 the brightness of 200cds/cm. The color coordinate was acquired for the luminescent color of x= 0.649 and y= 0.338, and optical ejection effectiveness improved 1.5 times as compared with the gestalt 1 of operation.
[0105]
[Effect of the Invention] As mentioned above, the OLED display of the active-matrix drive type which fits high-speed operation, can make the effect min, can make small fluctuation of the current value which flows to OLED, and obtains the high display engine performance by this invention even if there is property dispersion which makes the threshold of a transistor representation in the large large-sized high definition of wave delay or a display panel with a built-in circuit can be offered.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The circuit diagram of the pixel circuit of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 2] Drawing showing the drive wave of the pixel circuit of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 3] Drawing showing the drive wave of the pixel circuit of the conventional active-matrix mold OLED display
[Drawing 4] Drawing showing the equal circuit in each timing of the pixel circuit of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 5] Drawing showing the equal circuit in the 2nd timing of the pixel circuit of the conventional active-matrix mold OLED display
[Drawing 6] Drawing showing the operating point of the 1st transistor of the gestalt 1 of operation of this invention, and the pixel circuit of the conventional active-matrix mold OLED indicating equipment
[Drawing 7] The top view of the pixel of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 8] The sectional view of the pixel of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 9] Drawing showing the effectiveness over the gate propagation delay time of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 10] Drawing showing the effectiveness over threshold dispersion of the active-matrix mold OLED display of the gestalt 1 of operation of this invention
[Drawing 11] The circuit diagram of the pixel circuit of the active-matrix mold OLED display of the gestalt 2 of operation of this invention
[Drawing 12] Drawing showing the operating point of the 1st transistor of the gestalt 1 of operation of this invention, and the pixel circuit of the active-matrix mold OLED indicating equipment of an example 2
[Drawing 13] The circuit diagram of the pixel circuit of the active-matrix mold OLED display of the gestalt 3 of operation of this invention
[Drawing 14] Drawing showing the comparison of the OFF state current of the 2nd transistor of the gestalt 6 of operation of this invention
[Drawing 15] General drawing of the active-matrix mold OLED display of the gestalt 7 of operation of this invention
[Drawing 16] The whole vertical-scanning circuit circuit diagram of the gestalt 8 of operation of this invention
[Drawing 17] The circuit diagram of the bitblock_c part in drawing 16
[Drawing 18] The circuit diagram of the vbuffer_c part in drawing 17
[Drawing 19] The circuit diagram of the precharge circuit of the gestalt 9 of operation of this invention
[Drawing 20] Drawing showing the relation of the discernment marginal brightness and brightness of people
[Drawing 21] Drawing showing dispersion in the OLED current by fluctuation of lambda of the

gestalt 10 of operation of this invention
[Drawing 22] Drawing showing the channel length dependency of lambda of the gestalt 10 of operation of this invention
[Drawing 23] Drawing showing dispersion in the OLED current over the OFF state current of the 2nd transistor of the gestalt 10 of operation of this invention
[Drawing 24] The sectional view of the pixel of the active-matrix mold OLED display of the gestalt 13 of operation of this invention
[Drawing 25] The circuit diagram of the pixel circuit of the conventional active-matrix mold OLED display
[Description of Notations]
MDR The 1st transistor
MSH The 2nd transistor
MWR The 3rd transistor
MCH The 4th transistor
GL1 The 1st scanning line
GL2 The 2nd scanning line
GL3 The 3rd scanning line
DATA Signal line
VDD Power-source line
CS Capacitor for maintenance
31 Pixel Electrode (Anode Electrode)
22 OLED Layer
32 Cathode Electrode
AA Effective viewing area (usual picture area)
GD Built-in vertical-scanning circuit
PR Built-in precharge circuit
DT Video-signal end-of-line child
CT Cathode terminal
AT Anode terminal
LS Built-in level shift circuit

[Translation done.]

* NOTICES *

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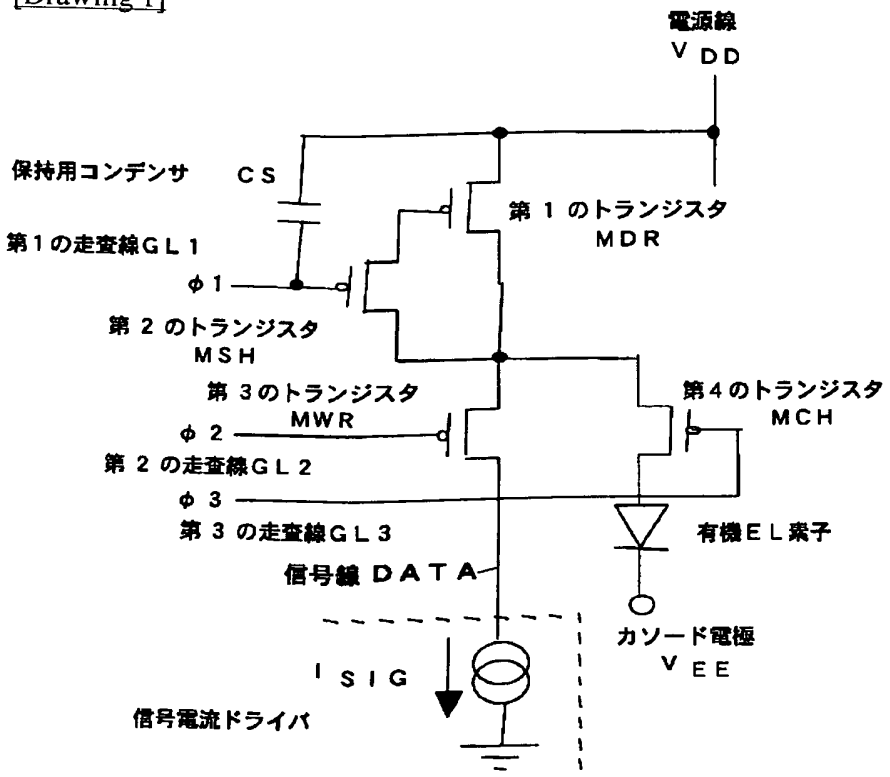
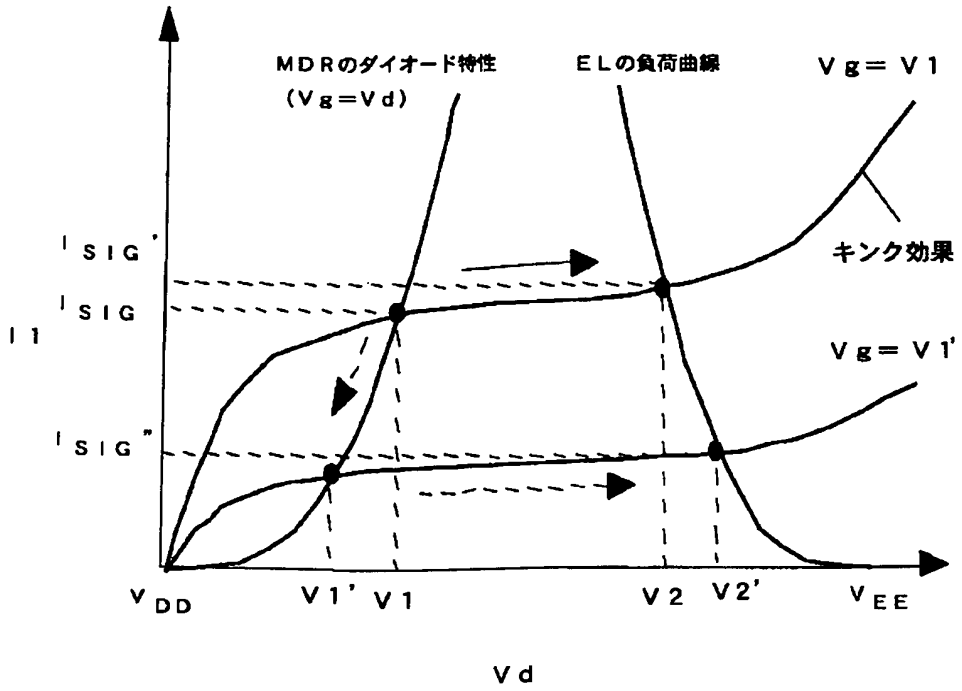
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

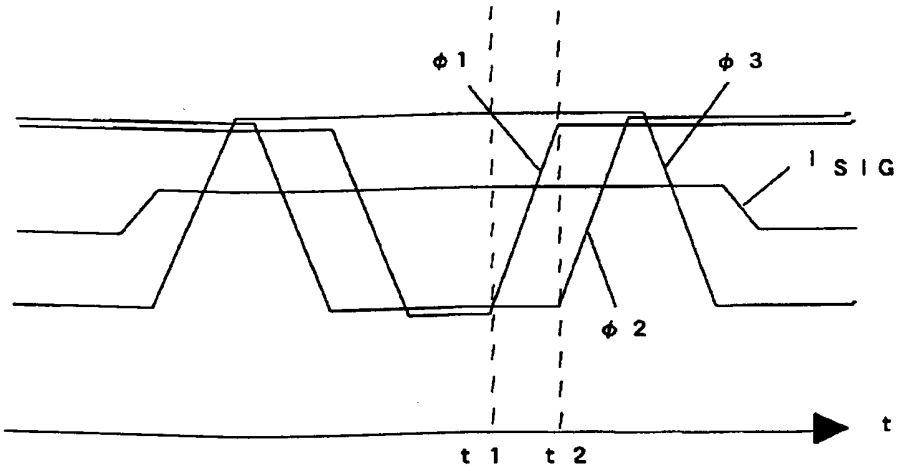
[Drawing 1]



[Drawing 6]


MDRのダイオード特性
(Vg=Vd)
ELの負荷曲線
Vg= V1
キンク効果
Vg= V1'
I SIG'
I SIG
I1
I SIG"
VDD
V1' V1
V2 V2'
VEE
Vd

[Drawing 2]



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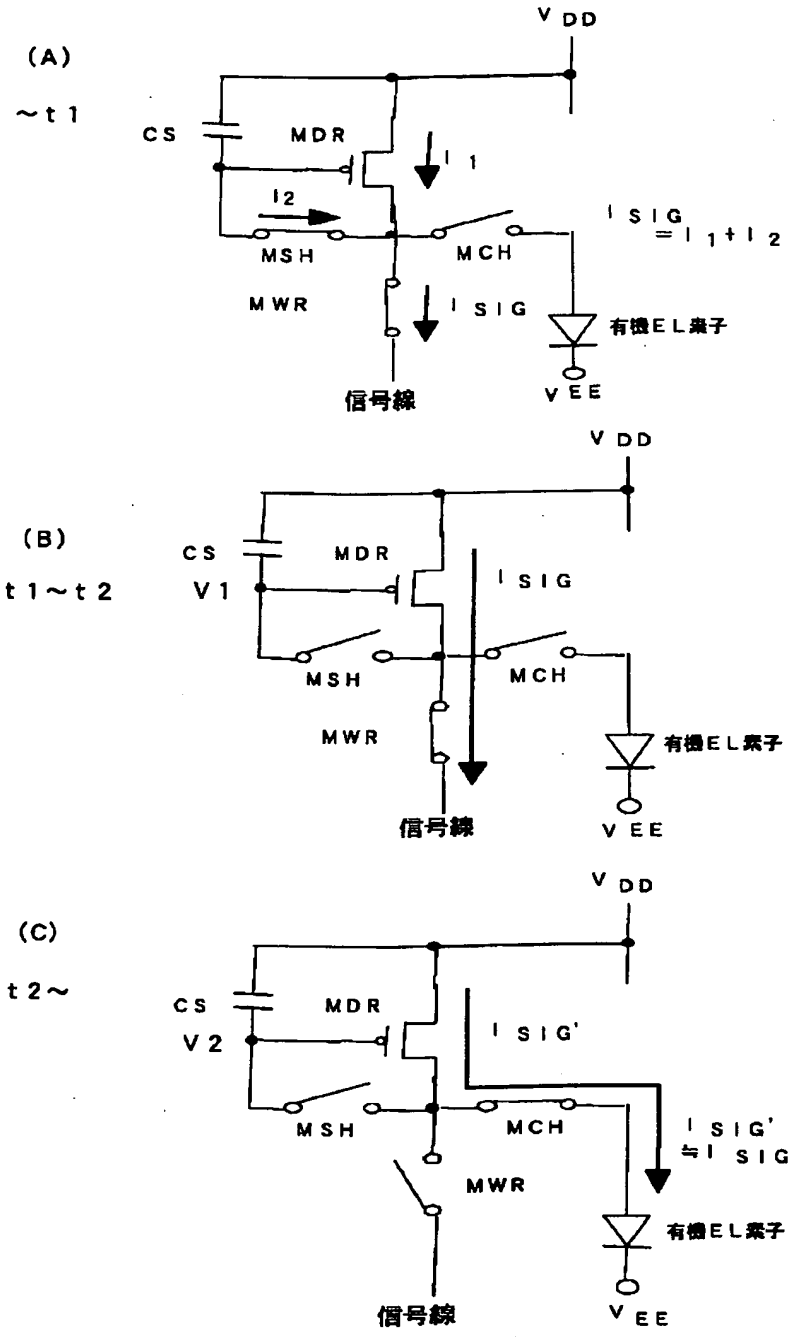
(A)
～t 1
V DD
CS
MDR
I 1
I2
I SIG
=I 1+I 2
MSH
MCH
MWR
I SIG
有機EL素子
信号線
V EE
(B)
t 1～t 2
V DD
CS
V1
MDR
I SIG
MSH
MCH
MWR
有機EL素子
信号線
V EE
(C)
t 2～
V DD
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≒I SIG
MWR
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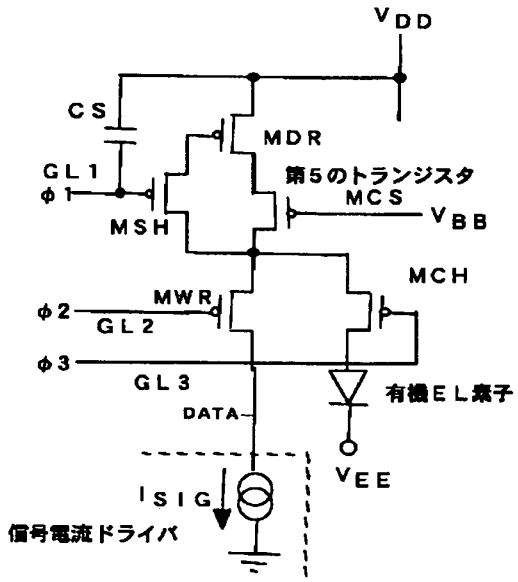
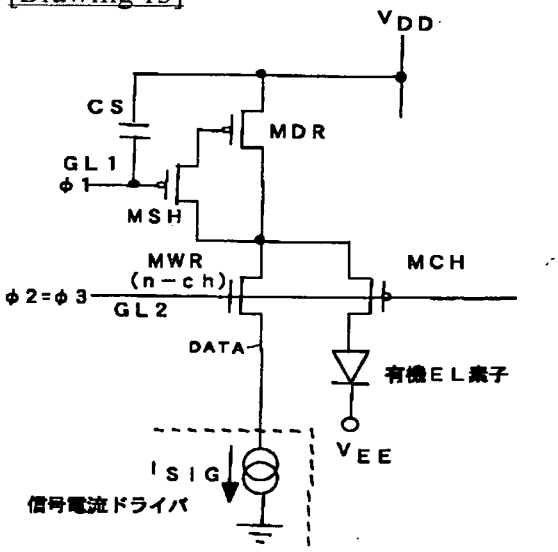
信号線
V EE

[Drawing 11]



[Drawing 13]



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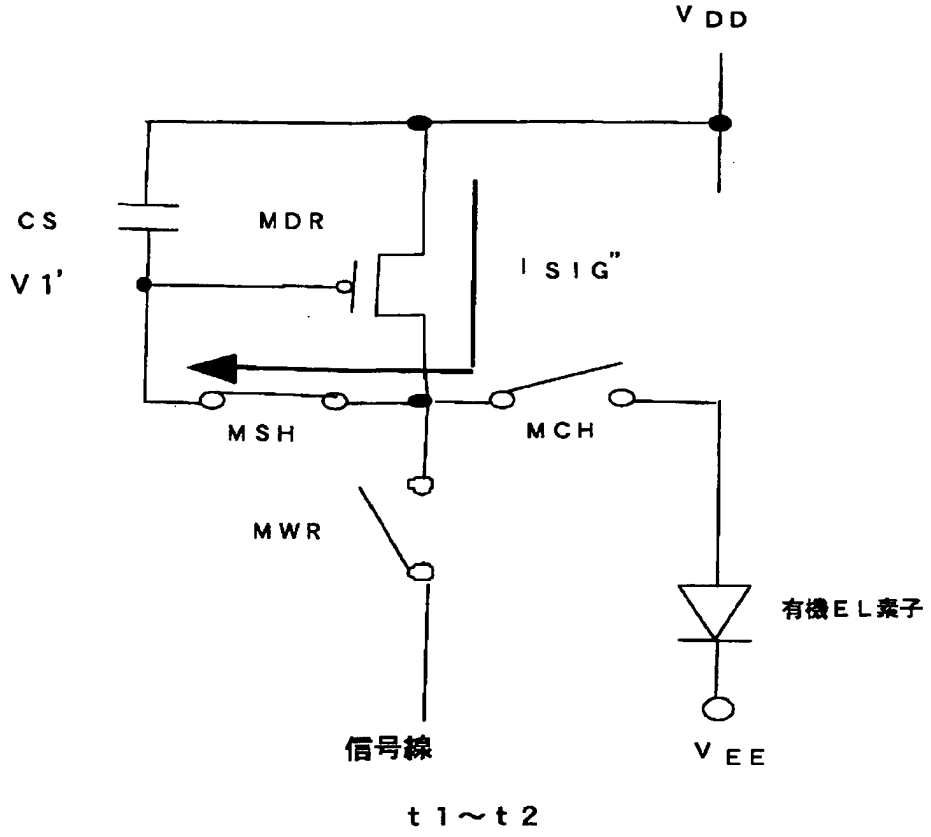

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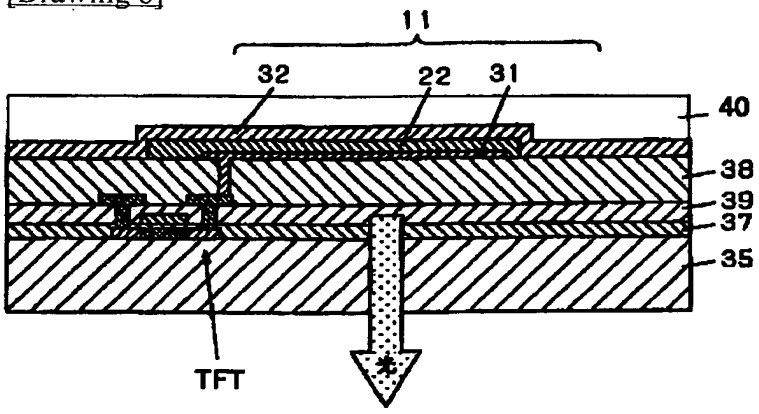

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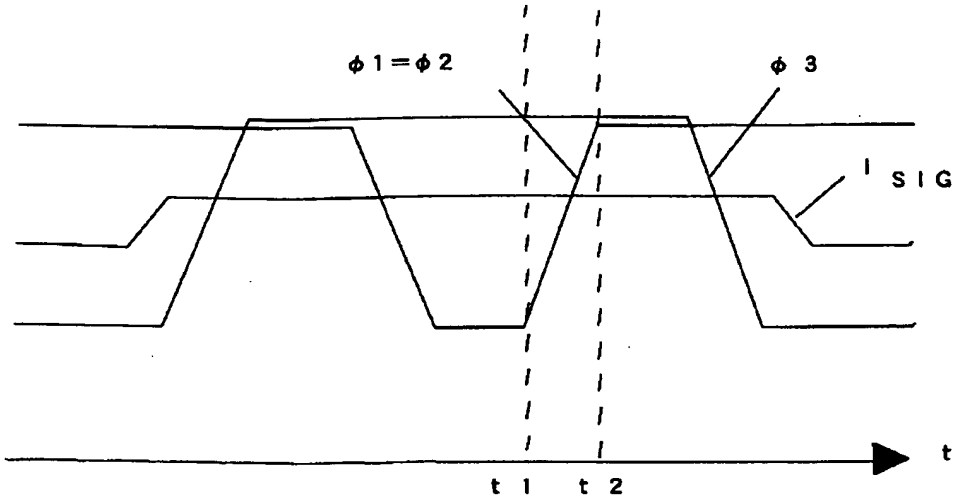

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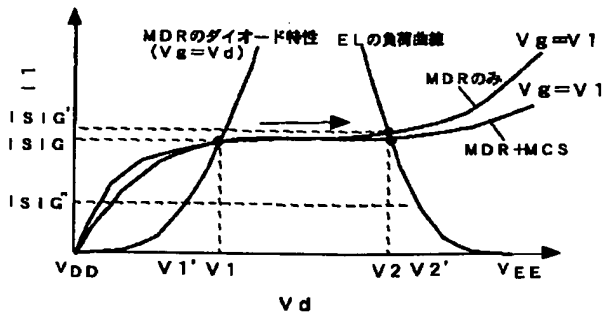

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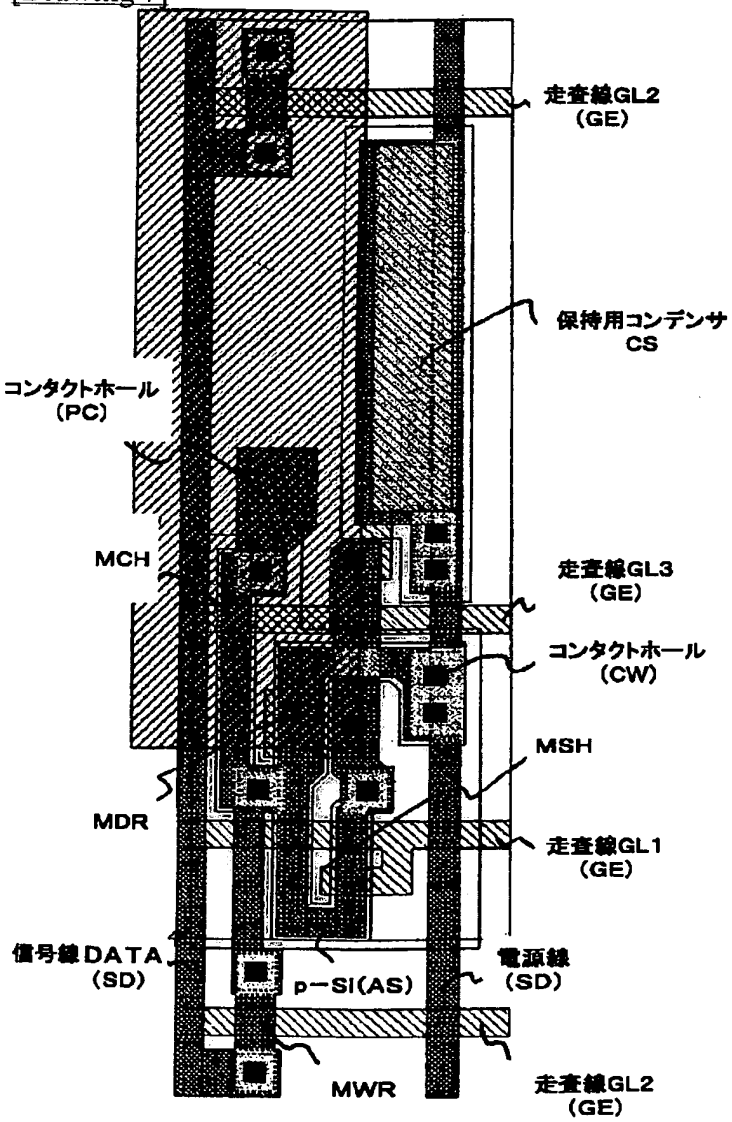

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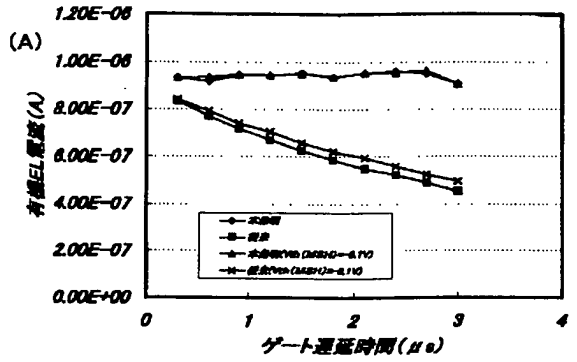

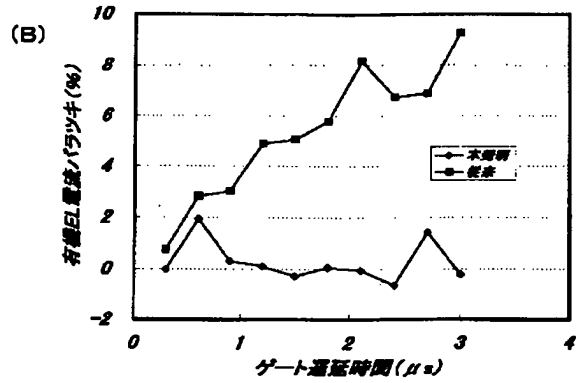

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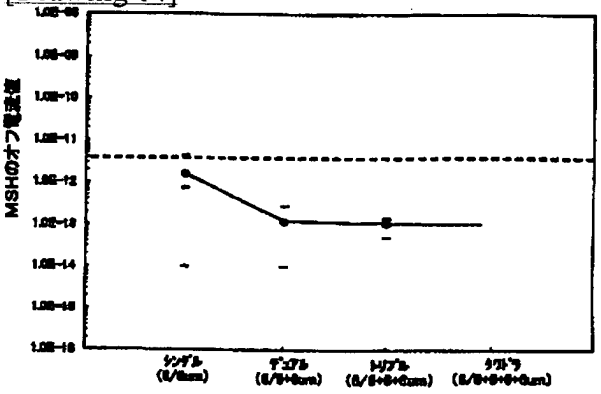

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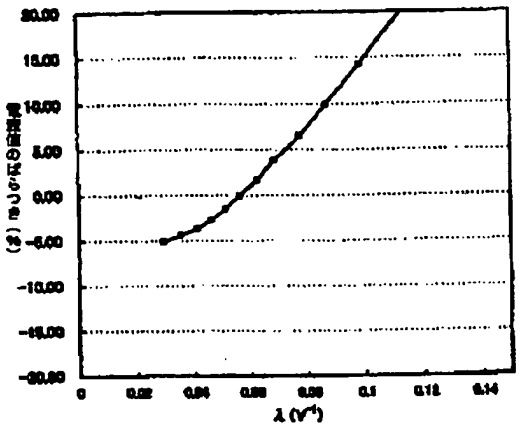

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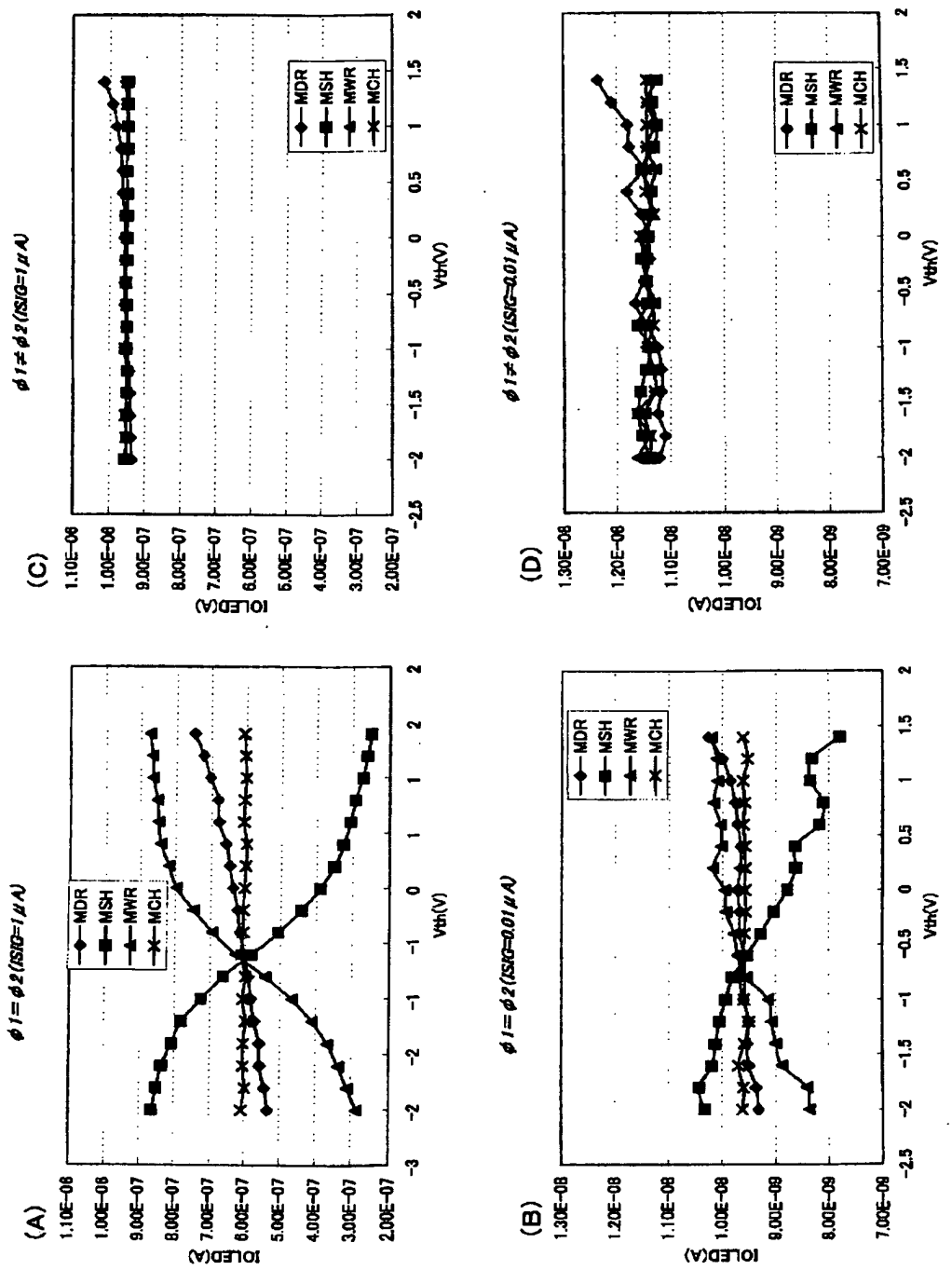

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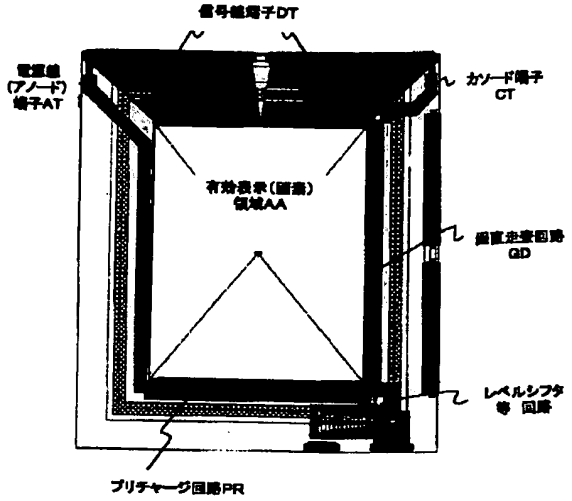

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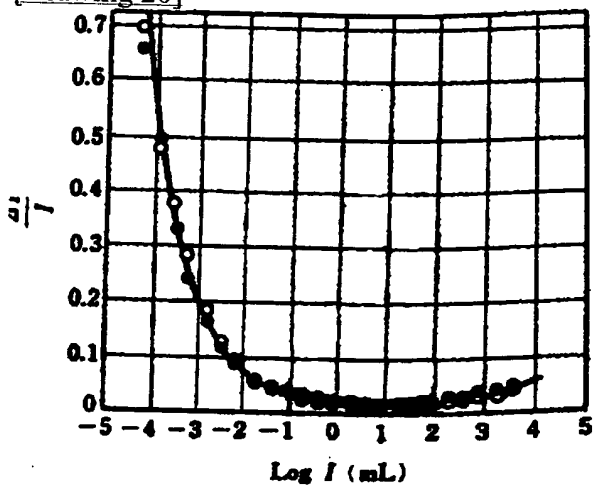

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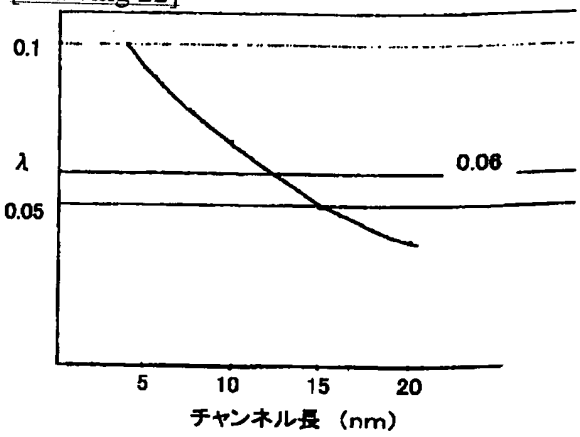

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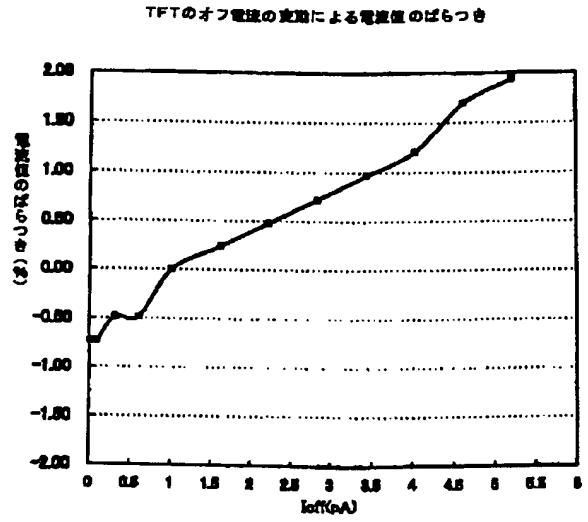
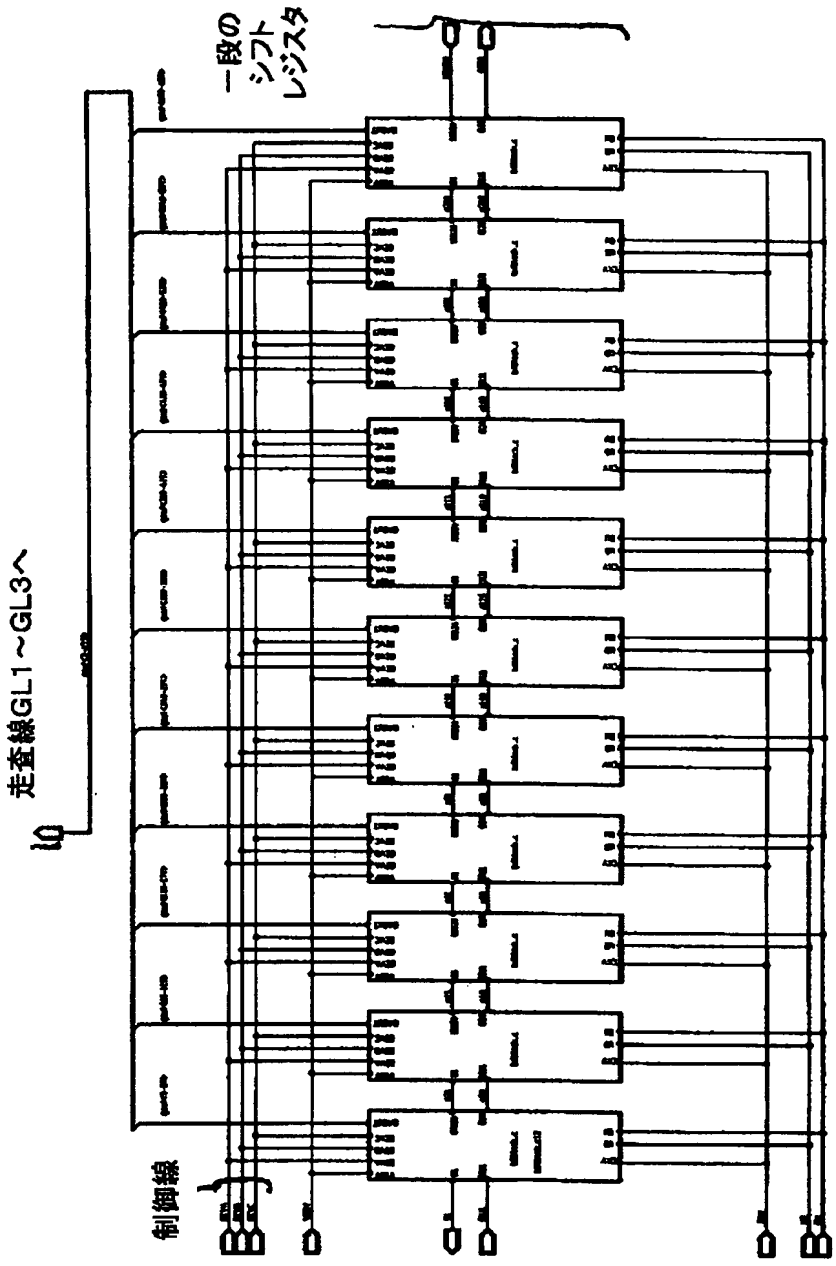

TFTのオフ電流の変動による電圧値のばらつき
2.00
1.50
1.00
0.50
0.00
-0.50
-1.00
-1.50
-2.00
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
5.5
6
Ioff(pA)

[Drawing 16]



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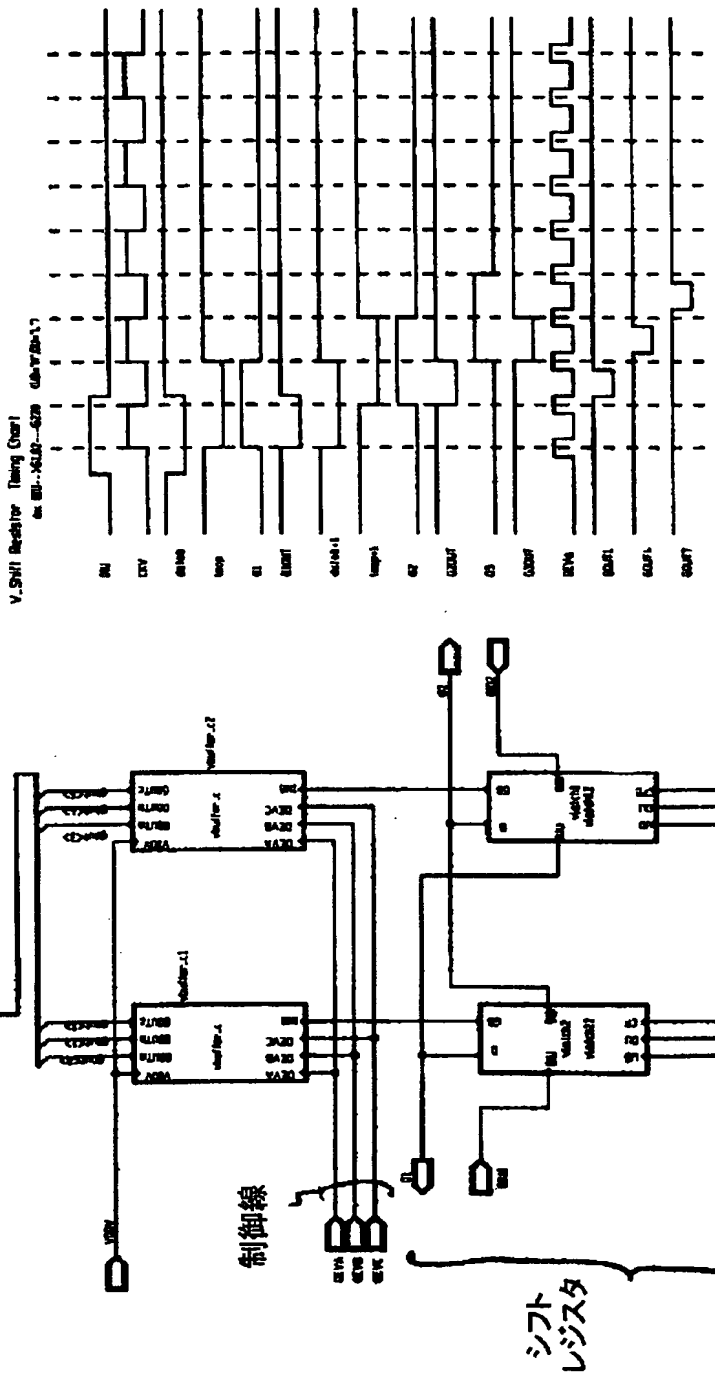

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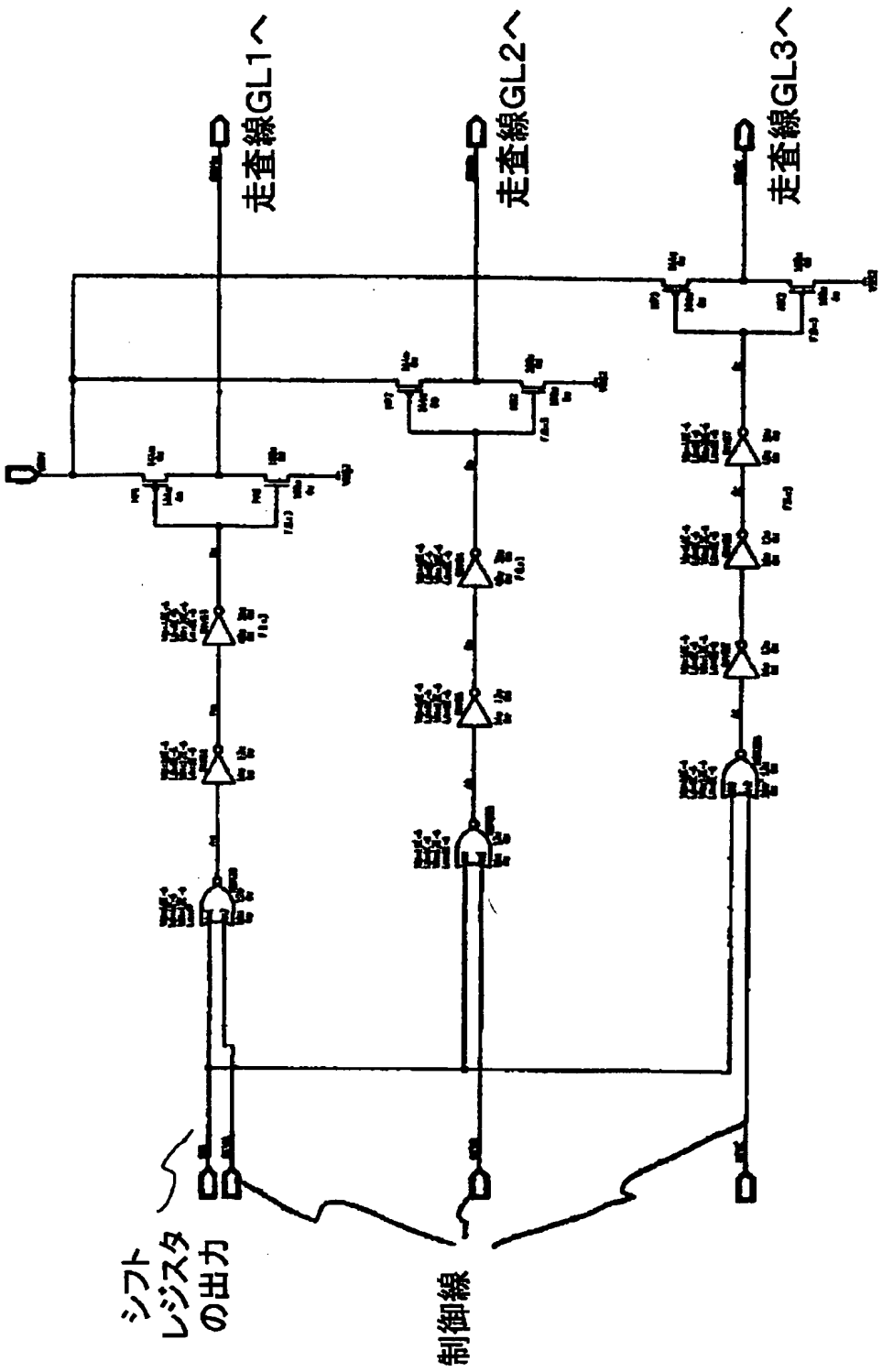

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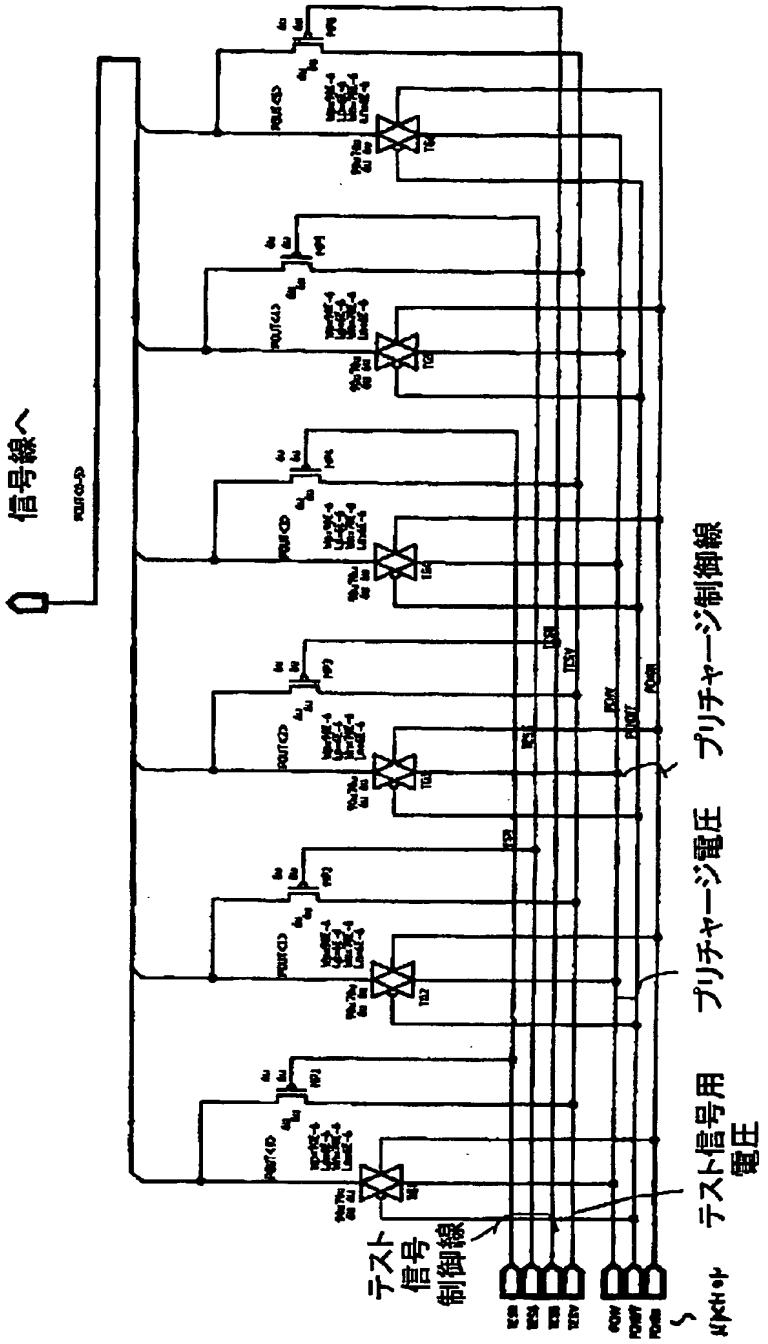

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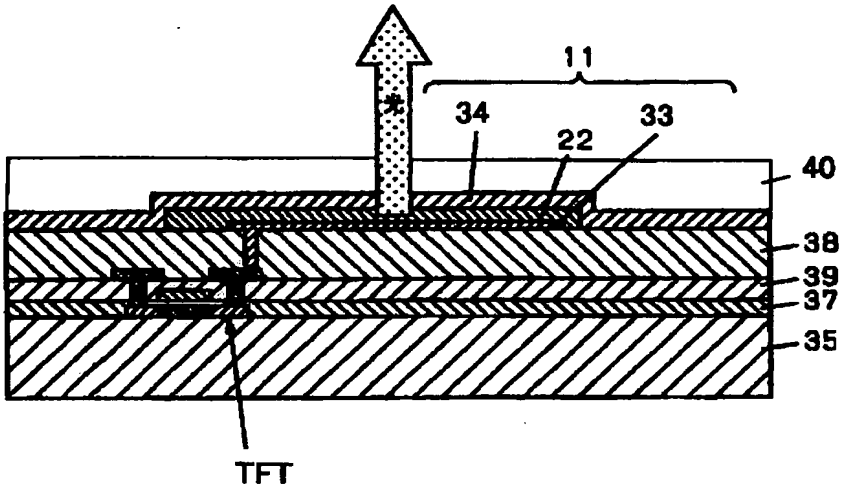

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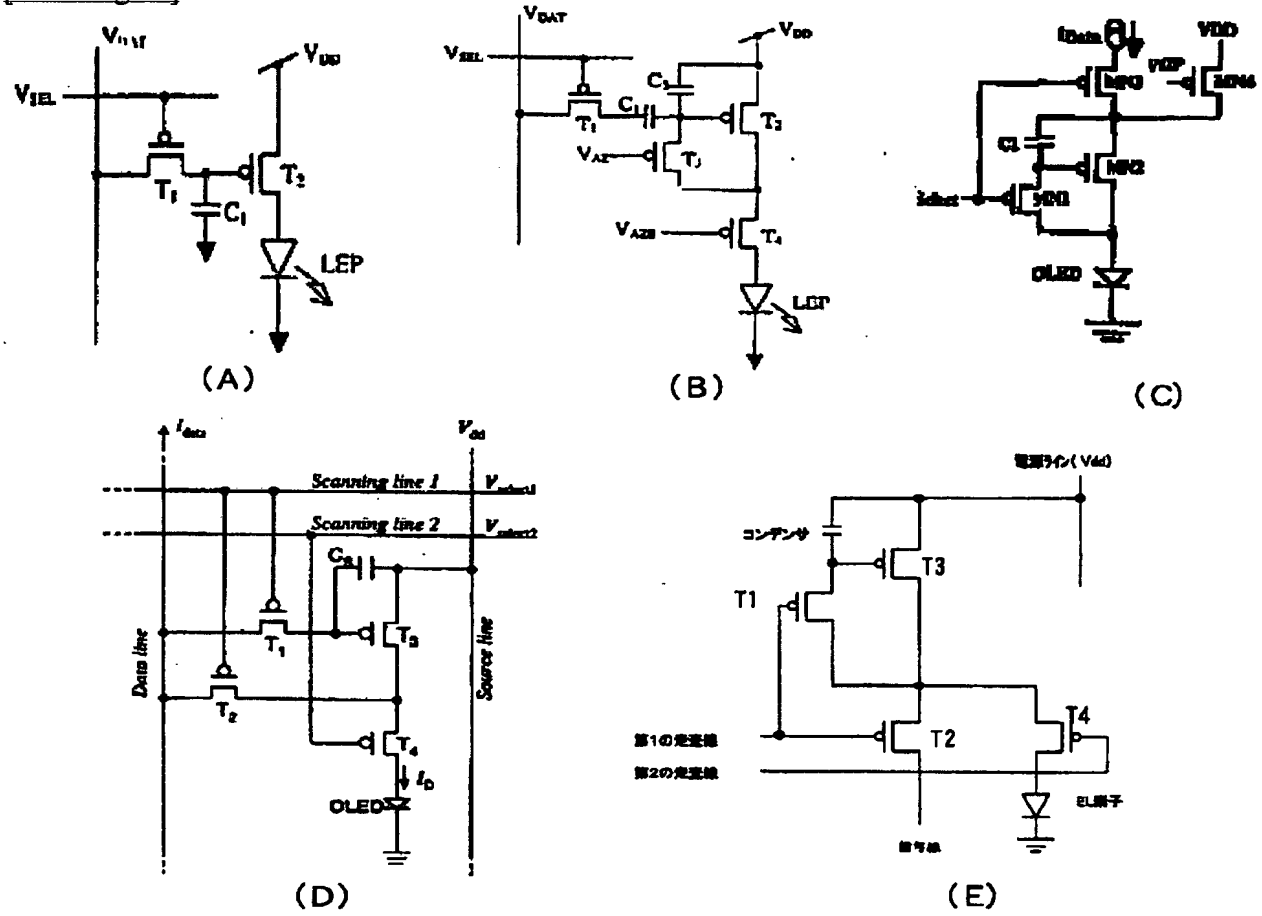

[Translation done.]